A New Test Pattern Generator for High Defect Coverage in a BIST Environment

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I. The Proposed TPG Design

In this paper we propose a new Test Pattern Generator (TPG) for the detection of realistic faults occurring in CMOS nanometer technologies (Fig. 1). The same TPG with a simple modification (Fig. 2) can be used for testing more than one modules in a SoC.

Main Characteristics

- Generation of low power test sequences
- Detection of design defects modeled as stuck-at or delay faults
- Single on-chip testing solution
- Cost effective solution with respect to area overhead for testing more than one modules in a SoC
- Very high defect efficiency for stuck-at, robust and non robust delay faults compared to previously proposed TPGs

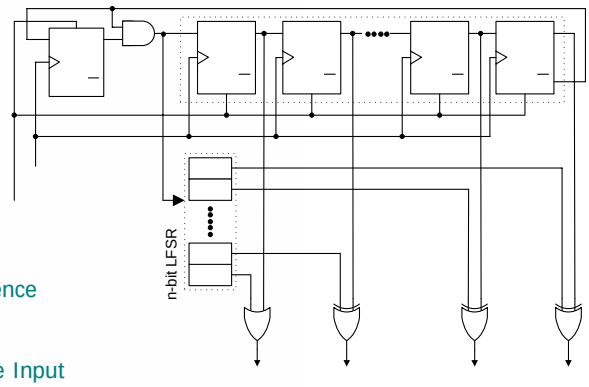


Figure 1

For each pseudorandom pattern produced by the LFSR, this scheme produces a sequence of 2n+1 Single Input Change (SIC) test vectors.

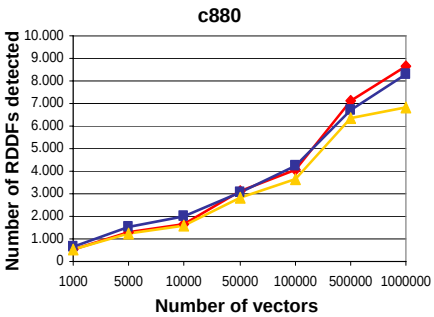
Between consecutive sequences of 2n+1 SIC test vectors the TPG generates a Multiple Input Change (MIC) pair of vectors.

II. Experimental Results

Delay Fault Testing

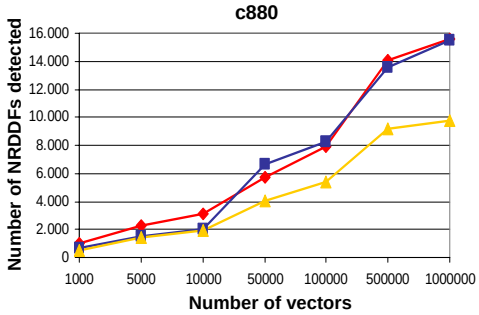
Robustly Detectable Delay Faults (RDDFs)

- The proposed TPG and (■) reach approximately the same level of fault efficiency
- The proposed TPG detects up to 26% more RDDFs than (■)



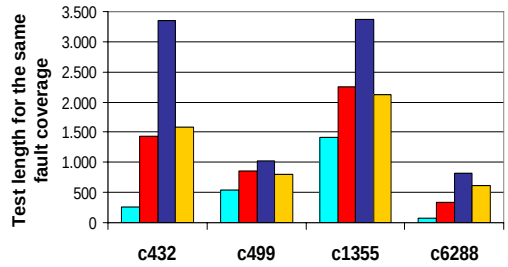
Non Robustly Detectable Delay Faults (NRDDFs)

- There is an increase up to 14% when the proposed TPG is used instead of (■)
- With the proposed TPG the number of NRDDFs detected can be more than twice the number detected by (■)



Stuck-At Fault Testing

- The efficiency of the proposed TPG and (■) are similar
- Test sequences required by (■) are always of greater length for the same fault coverage
- For circuits with many random pattern resistant faults, such as c2670 and c7552, the proposed TPG achieves higher fault coverage than (■)
- For test lengths equal to those used for delay fault testing the proposed TPG reaches the same level of efficiency with an LFSR



■ = LFSR ■ = Proposed TPG ■ = P. Girard et al. ■ = R. David et al.

III. Testing Several Modules Using the Same TPG

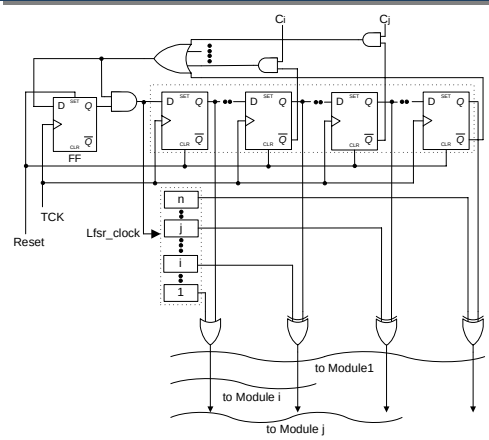


Figure 2

The TPG is designed in order to test an n-input module. For every extra module we wish to test an additional two-input AND gate is required. The outputs of the AND gates and signal Q_{bar} from the last stage of the Shift Register are the inputs of an OR gate. Signals Ci, ..., Cj, generated by the BIST controller, determine which module is tested each time. At most only one of the signals Ci, ..., Cj will have the value 1 each time.

- When Ci=...=Cj=0 then Module1 is tested
- When Cj=1 then Module j is tested

With this modification the proposed TPG:

- is a reduced area overhead solution for testing several modules one by one
- reaches the same level of fault efficiency with that of a dedicated TPG exclusively designed for testing each specific module
- is applicable in the case of a SoC with several buses of different size each one

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