A Synchronization Scheme for Single-Phase Grid-Tied Inverters under Harmonic Distortion and Grid Disturbances

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***Abstract*—Synchronization is a crucial aspect in grid-tied systems, including single-phase photovoltaic inverters, and it can affect the overall performance of the system. Among prior-art synchronization schemes, the Multi Harmonic Decoupling Cell Phase-Locked Loop (MHDC-PLL) presents a fast response under grid disturbances and high accuracy under harmonic distortions. However, major drawbacks of the MHDC-PLL include increased complexity and inaccurate response under non-nominal frequencies, which may occur in practical applications. Thus, this paper proposes strategies to address these issues. At first, a novel re-formulation of an equivalent decoupling cell is proposed for reducing the implementation complexity, and then a frequency adaptive quadrature signal generator for the MHDC-PLL is proposed to enable an accurate response even under non-nominal frequencies. Simulation and experimental results are provided, which show that the proposed synchronization (i.e., the frequency adaptive MHDC-PLL) can achieve a fast and accurate response under any grid disturbance and/or severe harmonic conditions.**

Keywords—grid tied inverter; harmonic distortion; phase locked loop; photovoltaics; synchonization.

I. INTRODUCTION

The integration of roof-top photovoltaic (PV) systems has rapidly increased in recent years, where a single-phase configuration is preferable. Such single-phase PV systems employ grid-side power electronic inverters to properly inject the produced energy into the power grid [1], as it is exemplified in Fig. 1. The inverter controller ensures a proper operation of the grid-tied PV systems [1]-[5]. The inverter controller is based on a synchronization unit, an active (*P*) and reactive (Q) power controller, a current controller and a Maximum Power Point Tracker (MPPT). As shown in Fig. 1, the synchronization unit is a crucial part of the inverter controller, since it can affect the inverter controllers and as a result the entire system operation.

The synchronization unit is usually performed by a Phase-Locked Loop (PLL) algorithm and it is responsible for a fast and accurate estimation of the grid voltage and phase angle at the Point of Common Coupling (PCC) under any grid condition (e.g., voltage sags). A fast synchronization enables a proper dynamic performance of the inverter, which is essential for providing Fault Ride Through (FRT) support under low-voltage grid faults that is required by the grid regulations [6], [7]. It should be noted that Japan [8] and Italy [9] have already issued FRT regulations even for single-phase inverters. Moreover, the accuracy of the synchronization against voltage harmonic distortions can benefit the power quality of the PV system as discussed in [10]. Thus, it is vital to propose an advanced PLL scheme in terms of fast and good dynamic response under grid faults as well as high robustness against harmonics in these applications.

In the prior-art work, several advanced PLL-based synchronization methods can be found. An Inverse Park Transformation (IPT) based PLL [11], [12] and synchronization based on adaptive filtering and generalized integrators, such as the Enhanced PLL (EPLL) [2], [12] and the Second Order Generalized Integrator (SOGI-PLL) [12], [13] respectively, present fast dynamic responses. However, the performance of these PLL schemes is poor under low-order voltage harmonic distortions. It is more often to observe such performance degradation in the EPLL. In order to improve the robustness against low-order harmonic distortions, synchronization techniques based on adaptive or notch filtering techniques [14], [15], solutions using repetitive and multi-resonant controllers [16], and schemes based on moving average filters [17], [18] have been proposed. Nevertheless, the harmonic robustness of these methods is achieved at the cost of the dynamic response of the corresponding synchronization.

An interesting PLL scheme is proposed in [19], [20] based on a novel Multi Harmonic Decoupling Cell (MHDC) PLL,

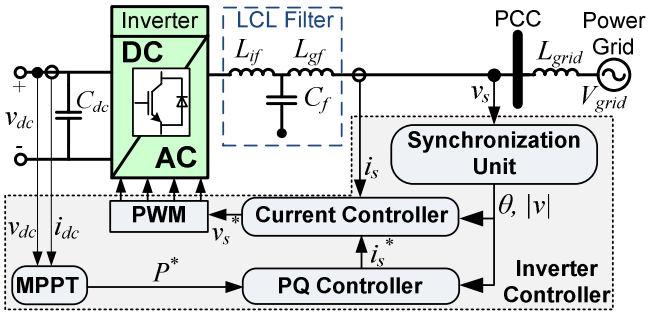

Fig. 1. Structure of a grid-tied inverter and its controller with a synchronization unit.

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which can achieve an accurate performance under harmonic distortions without affecting its dynamic responses. Major disadvantages of the MHDC-PLL are, however, the increased complexity in terms of heavy computation burden and the inaccurate response under non-nominal frequencies (e.g., a frequency jump).

This paper aims to address these major issues and thus to improve the performance of the MHDC-PLL by proposing a frequency adaptive MHDC-PLL. In Section II.A, a frequency adaptive Quadrature Signal Generator (QSG) is developed to enable an accurate response under non-nominal frequencies. In Section II.B, the MHDC is reformulated in such way to achieve an equivalent fast and accurate performance under harmonic distortion and grid disturbances, but with a decrease in complexity and required processing time. Finally, in Section II.B, the development of the frequency adaptive MHDC-PLL is proposed. A performance analysis and a complexity assessment of the proposed synchronization scheme is performed in Section III, while Section IV demonstrates simulation and experimental results of the frequency adaptive MHDC-PLL. Finally, conclusions are drawn in Section V.

II. Frequency Adaptive MHDC-PLL

The MHDC-PLL proposed in [19], [20] employs a Quadrature Signal Generator (QSG) unit to generate the in-quadrature voltage vector ($\mathbf{v}_{\alpha\beta}$) that is free of high-order harmonics, the MHDC to dynamically decouple the effect of low-order harmonics, and the *dq*-PLL algorithm to estimate the phase angle of the fundamental voltage component ($\mathbf{v}^{+1}$). The MHDC-PLL of [19], [20] suffers from the increased implementation complexity of the MHDC and the non-ideal or unsatisfactory responses of the QSG under frequency changes as mentioned in [13]. Hence, the following propose schemes to address these issues.

A. Frequency Adaptive Quadrature Signal Generator

The QSG of the MHDC-PLL in [19], [20] is based on a combination of an Inverse Park Transformation (IPT) method for cancelling the high-order harmonics and on a $T/4$ delay unit, where T is the period of the grid voltage, to generate the in-quadrature voltage vector. The IPT method is based on a forward Park's transformation, on a low-pass filter $\omega_{f1}/(s+\omega_{f1})$, and on a backward Park's transformation as described in [19]. It should be noted that the IPT method is not used for the in-quadrature vector $v_{\alpha\beta}$ generation, since the filtering effect of IPT on v_α and v_β is different. Thus, a more complicated design of the MHDC is required for cancelling out the low-order harmonics. Here, the IPT is only used for filtering the high-order harmonics of the grid voltage v_s. Therefore, the v_α is free of high-order harmonics and then a T/4 delay unit is used for generating the in-quadrature voltage vector $\mathbf{v}_{\alpha\beta}$.

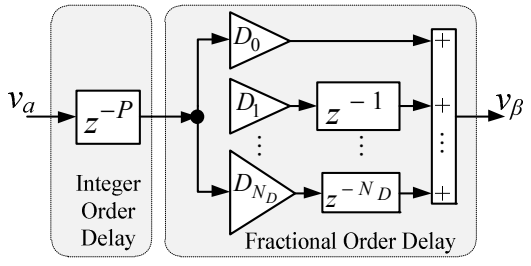

Fig. 2. Structure of the proposed frequency adaptive MHDC-PLL.

The $T/4$ delay unit of [19], [20] can accurately be performed in a digital controller, only when the ratio between the sampling rate (f_s) and the grid frequency (f_{grid}) is an integer. Thus, in the case where the ratio ($f_s/4 \cdot f_{grid}$) is an integer, the in-quadrature voltage vector $\mathbf{v}_{\alpha\beta}$ can equivalently be expressed in the continuous and in the discrete-time domains as,

$$\begin{aligned}\text{Continuous-time} \rightarrow \mathbf{v}_{\alpha\beta}(t) &= \begin{bmatrix} v_a(t) \\ v_\beta(t) \end{bmatrix} = \begin{bmatrix} v_a(t) \\ v_\alpha(t - T/4) \end{bmatrix} \\ \text{Discrete-time} \rightarrow \mathbf{v}_{\alpha\beta}(k) &= \begin{bmatrix} v_a(k) \\ v_\beta(k) \end{bmatrix} = \begin{bmatrix} v_a(k) \\ v_\alpha(k - f_s/4\, f_{grid}) \end{bmatrix}\end{aligned} \tag{1}$$

Unfortunately, in the case where the ratio ($f_s/4 \cdot f_{grid}$) is not an integer, the $T/4$ delay unit of [19], [20] can only approach the closest sample ($k_{T/4}$) to the $T/4$ delayed signal, where $k_{T/4}$ is the rounded $f_s/(4 \cdot f_{grid})$. Hence, when the grid frequency varies, the generated discrete-time $v_\beta(k)$ can present a phase shift error $\Delta\varphi$ from its desired continuous-time signal $v_\beta(t)$ as explained by,

$$v_\beta(k) = v_\alpha(k - k_{T/4}) \Leftrightarrow v_\beta(t) = v_\alpha(t - T/4 \pm \Delta\varphi) \tag{2}$$

In the worst case scenario, the phase error $\Delta\varphi$ is equal to $180 f_s/f_{grid}$. For instance, when f_s=10 kHz, the phase error can reach 0.89 degrees, when f_{grid}=49.505 Hz. Such a phase shift error on the in-quadrature voltage vector $\mathbf{v}_{\alpha\beta}$ will cause significant oscillations on the voltage signals expressed in the synchronous reference frame. As a result, undesired inaccuracies on the synchronization signals will be raised. A straight forward way to overcome this issue is to use a variable sampling rate as discussed in [21] to ensure that the $f_s/(4 \cdot f_{grid})$ is always an integer under any grid frequency. However, in such grid-tied inverter applications, the variable sampling rate is usually not an option, due to several restrictions on the controller design.

Hence, a novel frequency adaptive implementation of the $T/4$ delay unit is introduced in the following to enable an accurate operation of the MHDC-PLL under any grid frequency. The proposed frequency adaptive $T/4$ delay unit is developed in a digital controller by splitting the $T/4$ delay unit (i.e., $z^{-(f_s/f_{grid})/4}$) into an integer order delay (z^{-P}) and a fractional order delay (z^{-F}) as shown in Fig. 2. Then, the fractional order delay (z^{-F}) is approximated using the *Langrange* interpolation polynomial finite-impulse-response filter [22] as,

$$\begin{aligned} z^{-(f_s/f_{grid})/4} &= z^{-(P+F)} \\ \text{where:}\quad z^{-P} &= {}^{\text{Integer Order}}_{\text{Delay}}, \; z^{-F} \approx \sum_{l=0}^{N_D} D_l \cdot z^{-l}; \\ D_l &= \prod_{\substack{i=0 \\ i \neq l}}^{N_D} \frac{F-i}{l-i} \quad \text{and } l = 0,1,2...,N_D \end{aligned} \tag{3}$$

with N_D being the *Langrange* interpolation polynomial order, and N_D=3 being selected in this paper.

Such an adaptive $T/4$ delay unit according to (3) and Fig. 2 is then employed in the digital controller in order to generate the in-quadrature voltage vector $\mathbf{v}_{\alpha\beta}$. The discrete-time $v_\beta(k)$

can accurately estimate the continuous-time $v_\beta(t)=v_\alpha(t-T/4)$ due to the *Langrange* interpolation and thus, the use of the adaptive $T/4$ delay on the structure of the proposed frequency adaptive MHDC-PLL (as shown in Fig. 3) can enable an accurate synchronization at any grid frequency.

B. Reformulation of the MHDC for Complexity Reduction

The decoupling network (MHDC) of [19], [20] can achieve a dynamic cancellation of the low-order voltage harmonics and hence a fast and accurate synchronization can be ensured under any grid conditions (i.e., grid faults, high harmonic distortion). Another major disadvantage of the MHDC of [19], [20] is the increased complexity (processing burden) of the decoupling network, which may be sufficiently high in such real-time applications. Hence, a re-formulation of the decoupling network is proposed in the following in order to minimize the required processing time of the algorithm and still to achieve an exact equivalent response with the conventional MHDC [19], [20]. The complexity minimization is achieved by re-designing the decoupling network in the stationary reference frame ($\alpha\beta$-frame) instead of performing this in each synchronous reference frame (dq^n-frame) as it has initially been proposed in [19], [20].

The re-design of the decoupling network for dynamically cancelling out the low-order harmonics requires the analysis of the grid voltage under high harmonic distortion. As already proved in [19], the QSG is filtering out only the high-order harmonics (due to the IPT) and then it generates the v_β component by delaying the v_α for a period of $T/4$. Thus, under harmonic distorted conditions, the vector $\mathbf{v}_{\alpha\beta}$ can be expressed as a summation of the fundamental component (n=1) and of the low-order harmonics (n=3, 5, 7, 9, 11, 13, …), as given by,

$$\mathbf{v}_{\alpha\beta}=\mathbf{v}^1_{\alpha\beta}+\mathbf{v}^3_{\alpha\beta}+\mathbf{v}^5_{\alpha\beta}+\ldots=V^1\begin{bmatrix}\cos(\omega t+\theta_1)\\ \cos(\omega(t-\frac{\mathrm{T}}{4})+\theta_1)\end{bmatrix}+\sum_{n=3,5,7,\ldots}V^n\begin{bmatrix}\cos(n\omega t+\theta_n)\\ \cos\left(n\omega(t-\frac{\mathrm{T}}{4})+\theta_n\right)\end{bmatrix}, \tag{4}$$

where V^n and θ_n represent the amplitude and the initial phase angle of each voltage component respectively and ω is the angular grid frequency. Based on the QSG of the MHDC-PLL [19], [20] and by using basic trigonometric identities, (4) can be analyzed into,

$$\mathbf{v}_{\alpha\beta}=\sum_{n=1,3,5,7,\ldots}\mathbf{v}^n_{\alpha\beta}=\sum_{n=1,3,5,7,\ldots}V^n\begin{bmatrix}\cos(\mathrm{sgn}(n)\cdot n\omega t+\theta_n)\\ \sin\left(\mathrm{sgn}(n)\cdot n\omega t+\theta_n\right)\end{bmatrix} \tag{5}$$

$$\text{where}\quad \mathrm{sgn}(n)=\sin\left(\frac{n\pi}{2}\right)=\begin{cases}+1 & \text{for}\quad n=1,5,9,13,\ldots\\ -1 & \text{for}\quad n=3,7,11,\ldots\end{cases}$$

where sgn(n) defines the speed direction of each component. It worth noticing that the sgn(n) is inserted in this analysis due to the QSG-based $\mathbf{v}_{\alpha\beta}$.

According to (5) the direct calculation of each voltage component $\mathbf{v}^n_{\alpha\beta}$ is not possible due to the coupling effect among the existing components. However, an accurate estimation especially of the fundamental voltage component $\mathbf{v}^1_{\alpha\beta}$ is necessary for the grid synchronization of a grid-tied inverter and thus, a novel decoupling network is proposed hereafter. The development of the decoupling network requires to express (5) in terms of any voltage component $\mathbf{v}^n_{\alpha\beta}$ as,

$$\mathbf{v}^n_{\alpha\beta}=\mathbf{v}_{\alpha\beta}-\sum_{m\neq n}\mathbf{v}^m_{\alpha\beta}\Leftrightarrow\begin{bmatrix}v^n_\alpha\\ v^n_\beta\end{bmatrix}=\begin{bmatrix}v_\alpha\\ v_\beta\end{bmatrix}-\sum_{m\neq n}\begin{bmatrix}v^m_\alpha\\ v^m_\beta\end{bmatrix}\Leftrightarrow \tag{6}$$

Now, since the vectors $\mathbf{v}^m_{\alpha\beta}$ are unknown, the estimation of the voltage component $\mathbf{v}^n_{\alpha\beta}$ by $\mathbf{v}^{*n}_{\alpha\beta}$ is enabled in (7) by replacing the unknown vectors $\mathbf{v}^m_{\alpha\beta}$ of (6) with the corresponding filtered estimation vectors $\bar{\mathbf{v}}^{*m}_{\alpha\beta}$.

$$\mathbf{v}^{*n}_{\alpha\beta}=\mathbf{v}_{\alpha\beta}-\sum_{m\neq n}\bar{\mathbf{v}}^{*m}_{\alpha\beta} \tag{7}$$

The filtered estimation vectors $\bar{\mathbf{v}}^{*m}_{\alpha\beta}$ are produced by filtering out the corresponding estimation vector $\mathbf{v}^{*m}_{\alpha\beta}$ in order to eliminate any remaining oscillations after subtracting the coupling effect caused by the existence of other harmonic components. Since each estimation vector $\mathbf{v}^{*m}_{\alpha\beta}$ is rotated with a different sgn(m)·m·ω, an equivalent filtering cannot be directly achieved for each component. Therefore, for an equivalent filtering of all the voltage components, it is first necessary to express each estimated vector $\mathbf{v}^{*m}_{\alpha\beta}$ into a corresponding synchronous reference frame rotating with a sgn(m)·m·ω speed ($dq^{\mathrm{sgn}(m)m}$-frame) by using Park's transformation theory. Thus, the m component of the estimation voltage vector expressed in the corresponding $dq^{\mathrm{sgn}(m)m}$-frame ($\mathbf{v}^{*m}_{\mathbf{dq}^{\mathbf{sgn}(m)\boldsymbol{m}}}$) is given by,

$$\mathbf{v}^{*m}_{\mathbf{dq}^{\mathbf{sgn}(m)\boldsymbol{m}}}=\begin{bmatrix}v_{d\,\mathrm{sgn}(m)\cdot m}\\ v_{q\,\mathrm{sgn}(m)\cdot m}\end{bmatrix}=\left[T_{dq^{\mathrm{sgn}(m)\cdot m}}\right]\mathbf{v}^{*m}_{\alpha\beta} \tag{8}$$

$$\text{where}\quad\left[T_{dq^{\mathrm{sgn}(m)\cdot m}}\right]=\begin{bmatrix}\cos(\mathrm{sgn}(m)m\omega t) & \sin(\mathrm{sgn}(m)m\omega t)\\ -\sin(\mathrm{sgn}(m)m\omega t) & \cos(\mathrm{sgn}(m)m\omega t)\end{bmatrix}$$

It should be noted that each vector $\mathbf{v}^{*m}_{\mathbf{dq}^{\mathbf{sgn}(m)\boldsymbol{m}}}$ is actually described as a DC/non-rotating vector, since both the $dq^{\mathrm{sgn}(m)m}$-frame and the m voltage component are rotated with the same sgn(m)·m·ω speed. Therefore, an equivalent filtering can now be achieved since all the voltage components can be expressed as non-rotating vectors according to (8). Therefore, the filtered estimation vector $\bar{\mathbf{v}}^{*m}_{\mathbf{dq}^{\mathbf{sgn}(m)\boldsymbol{m}}}$ expressed in a corresponding $dq^{\mathrm{sgn}(m)m}$-frame is generated by filtering the corresponding estimation vector component $\mathbf{v}^{*m}_{\mathbf{dq}^{\mathbf{sgn}(m)\boldsymbol{m}}}$ according to,

$$\bar{\mathbf{v}}^{*m}_{\mathbf{dq}^{\mathbf{sgn}(m)\boldsymbol{m}}}=\begin{bmatrix}\bar{v}^{*m}_{d\ \mathrm{sgn}(m)m}\\ \bar{v}^{*m}_{q\ \mathrm{sgn}(m)m}\end{bmatrix}=\left[F(s)\right]\mathbf{v}^{*m}_{\mathbf{dq}^{\mathbf{sgn}(m)\boldsymbol{m}}} \tag{9}$$

$$\text{where}\quad\left[F(s)\right]=\frac{\omega_{f2}}{s+\omega_{f2}}\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}$$

and ω_{f2} is the cut-off frequency of the low-pass filter [$F(s)$] and should be set to $2\pi 50/3$ rad/s according to the theoretical analysis in [19]. Finally, the filtered estimation vector $\bar{\mathbf{v}}^{*m}_{\alpha\beta}$,

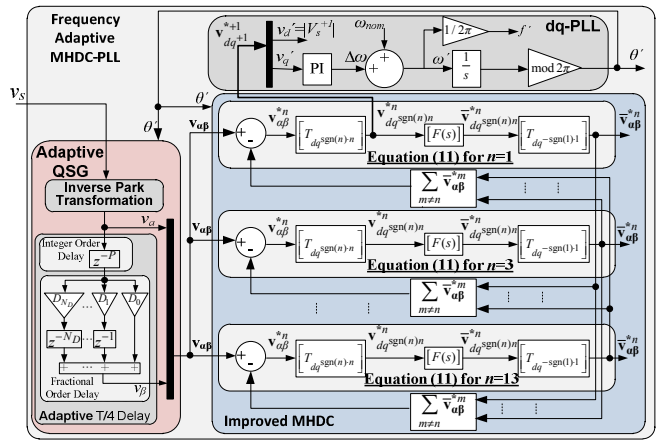

Fig. 3. Structure of the proposed frequency adaptive MHDC-PLL.

TABLE I. DESIGN PARAMETERS OF FREQUENCY ADAPTIVE MHDC-PLL

IPT unit	Filtering parameter → $\omega_{f1}=2\pi 50\sqrt{2}$ rad/s
Adaptive T/4 delay unit	*Langrange* interpolation order → $N_D=3$
Improved MHDC	Multiple use of (11) for n=1, 3, 5, 7 , 9, 11, 13 Filtering parameter → $\omega_{f2}=2\pi 50/3$ rad/s
dq-PLL	Tuning parameters → $k_P=92$, $T_I=0.000235$

required by (7) to develop the decoupling network, can be calculated based on Park's transformations and is given by,

$$\bar{\mathbf{v}}^{*m}_{\boldsymbol{\alpha\beta}} = \begin{bmatrix} \bar{v}^{*m}_{\alpha} \\ \bar{v}^{*m}_{\beta} \end{bmatrix} = \left[T_{dq^{-\mathrm{sgn}(m)\cdot m}} \right] \bar{\mathbf{v}}^{*m}_{\boldsymbol{dq^{\mathrm{sgn}(m)m}}} \tag{10}$$

When submitting (8) to (9) and then (9) to (10), (7) can be re-written as,

$$\mathbf{v}^{*n}_{\boldsymbol{\alpha\beta}} = \mathbf{v}_{\boldsymbol{\alpha\beta}} - \sum_{m\neq n} \left[T_{dq^{-\mathrm{sgn}(m)m}} \right] [F(s)] \left[T_{dq^{\mathrm{sgn}(m)m}} \right] \mathbf{v}^{*m}_{\boldsymbol{\alpha\beta}} \tag{11}$$

Finally, (11) is the cornerstone of the proposed decoupling network (improved MHDC) as shown in Fig. 3. Hence, the multiple use of (11) for n=1, 3, 5, 7, … in a cross feed-back decoupling network enables a dynamic estimation of each voltage component $\mathbf{v}^{*n}_{\boldsymbol{\alpha\beta}}$. It should be pointed out that the cross feed-back network is required to dynamically eliminate the coupling effect between the fundamental voltage component and all the significant low-order harmonic components. It is important to mention that the improved MHDC can achieve an exact equivalent performance with the MHDC in [19], [20], but the complexity of the improved MHDC is significantly decreased, as it will be proved in Section III.

C. Development of the Frequency Adaptive MHDC-PLL

The proposed frequency adaptive MHDC-PLL can now be developed based on the adaptive QSG (as described in Section II.A), the improved MHDC (as described in Section II.B) and on the *dq*-PLL algorithm [23] for estimating the phase angle of the grid voltage as shown in Fig. 3. The new frequency adaptive MHDC-PLL can achieve a fast and accurate synchronization under any grid disturbance and under highly harmonic distortion. The complexity of the synchronization has been significantly decreased compared to the MHDC-PLL of [19], [20], as it will be proved in Section III.

The adaptive QSG is based on the IPT method in order to filter out the high-order harmonics and then the proposed frequency adaptive T/4 delay unit is used to generate the voltage vector $\mathbf{v}_{\boldsymbol{\alpha\beta}}$. The proposed frequency adaptive method overcomes the inaccuracies under non-nominal frequency caused by the initial QSG used in [19], [20] and thus, an accurate operation can be achieved under any grid frequency.

Then, the $\mathbf{v}_{\boldsymbol{\alpha\beta}}$ is fed on the proposed improved MHDC as shown in Fig. 3, in order to dynamically cancel out the effect of the low-order harmonics with minimized computation burden. For a proper design of the improved MHDC, it is first necessary to define the number of harmonic-orders that are considered and eliminated by the decoupling network. An investigation is performed on the accuracy of the frequency adaptive MHDC-PLL under the worst-case voltage harmonic distortion according to EN50160 standards (see HC3 on Table II). The investigation shows that a very accurate synchronization (error in phase angle estimation $\theta_{error}=\theta_{grid}-\theta'$ less than 0.00035 rad) can be achieved, when the improved MHDC is designed for N=7, considering the fundamental (n=1) and the effect of the six most significant harmonic components (n=3, 5, 7, 9, 11, 13) in single-phase systems. The effect of the higher order harmonics is minimized due to the second-order band-pass filtering characteristics of IPT as mentioned in [19]. Therefore, the decoupling network of the frequency adaptive MHDC-PLL is designed for N=7 as shown in Fig. 3 in order to achieve an accurate synchronization under any harmonic distorted grid conditions. Thus, the fast and accurate estimation of the fundamental voltage component $\mathbf{v}^{*1}_{\boldsymbol{dq^{+1}}}$ expressed in the dq^{+1}-frame is enabled by the improved MHDC. This estimation voltage vector is free of any low- and high-order harmonics and therefore, the conventional dq-PLL algorithm can be used to accurately estimate the phase angle and the amplitude of the grid voltage, as demonstrated in Fig. 3.

The conventional dq-PLL system [23] is a closed-loop synchronization system, which aims to force the per unit $v'_q = v^{*1}_{q^{+1}}$ to track zero. The synchronization algorithm is based on a Proportional-Integral (PI) controller, whose transfer function is given by $k_p+1/(T_i s)$, with k_p and T_i being the controller parameters. Therefore, based on a linearized small signal analysis, the transfer function of the PLL is given by the second order transfer function of (12), where it is obvious that the tuning parameters (k_p and T_i) can affect the response of the synchronization unit.

$$\frac{\theta'}{\theta} = \frac{k_p \cdot s + 1/T_i}{s^2 + k_p \cdot s + 1/T_i} \tag{12}$$

where: $k_p = \dfrac{9.2}{ST}$ and $T_i = 0.047 \cdot \zeta^2 \cdot ST^2$

For an optimally damped response of the PLL, the damping coefficient ζ should be set to $1/\sqrt{2}$; the Settling Time (ST) has been set to 100 ms for the purposes of this work. Hence, the tuning parameters k_p and T_i of the frequency adaptive MHDC-PLL have been set to 92 and $2.35\cdot10^{-4}$, respectively.

The proposed frequency adaptive MHDC-PLL can achieve a fast and accurate response under any harmonic distortion and

under any grid faults and the required processing time of the proposed synchronization algorithm is significantly less compared to the original MHDC of [19], [20], as it will be demonstrated in Section III and IV. All the design parameters for developing the proposed frequency adaptive MHDC-PLL are summarized in Table I.

III. Performance Analysis - Complexity Evaluation

This section aims to prove that the proposed frequency adaptive MHDC-PLL (based on the improved MHDC) and the MHDC-PLL of [19], [20] can achieve an equivalent performance under any harmonic distorted grid voltage and that the proposed improved MHDC (Section II.B) requires significantly less processing time in each control loop.

The proposed improved MHDC, as shown in Fig. 3, is based on the multiple use of (11) for accurately estimating each voltage component. By analyzing (11), it can be proved that the improved MHDC can achieve an exact equivalent response with the original MHDC proposed in [19], [20]. Thus, by multiplying both sides of (11) with the transformation matrix $\left[T_{dq^{sgn(n)n}}\right]$ and applying Park's transformation theory, (11) can be equivalently re-written as (13).

$$\mathbf{v}^{*n}_{\boldsymbol{dq}^{\mathbf{sgn}(n)n}} = \left[T_{dq^{\mathrm{sgn}(n)n}}\right]\mathbf{v}_{\boldsymbol{\alpha\beta}} - \sum_{m\neq n}\left[T_{dq^{\mathrm{sgn}(n)n}}\right]\left[T_{dq^{-\mathrm{sgn}(m)m}}\right][F(s)]\mathbf{v}^{*m}_{\boldsymbol{dq}^{\mathbf{sgn}(m)m}} \quad (13)$$

Then, by filtering both side of (13) with the filtering matrix

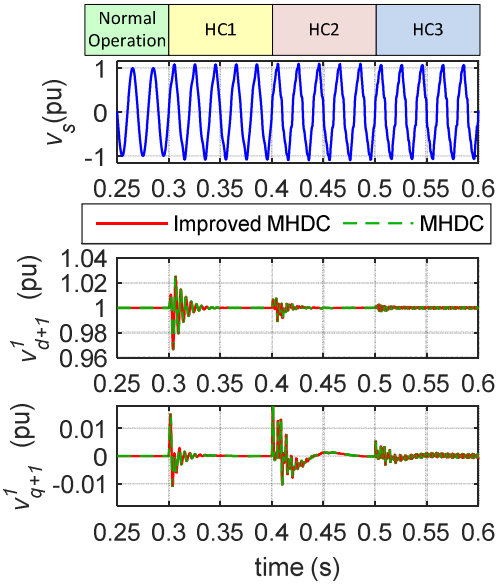

Fig. 4. Comparison of the performance of the proposed improved MHDC and of the MHDC of [19] and [20].

TABLE II. Definition of Several Harmonic Conditions (HC)

Normal Operation	Pure sinusoidal grid voltage
HC1	$\|V_3\|$=5% and $\|V_5\|$=6%
HC2	$\|V_3\|$=5%, $\|V_5\|$=6%, $\|V_7\|$=5%, $\|V_9\|$=1.5%, $\|V_{11}\|$=3.5%
HC3	Worst case harmonic distortion according to EN50160: $\|V_3\|$=5%, $\|V_5\|$=6%, $\|V_7\|$=5%, $\|V_9\|$=1.5%, $\|V_{11}\|$=3.5%, $\|V_{13}\|$=3%, $\|V_{15}\|$=0.5%, $\|V_{17}\|$=2%, $\|V_{19}\|$=1.5%, $\|V_{h>20}\|$=0.3%

$[F(s)]$, by using (9), and by merging the transformation matrices, (13) can be re-written as (14), which is the cornerstone equation of MHDC according to [19], [20].

$$\bar{\mathbf{v}}^{*n}_{\boldsymbol{dq}^{\mathbf{sgn}(n)n}} = [F(s)]\left\{\mathbf{v}_{\boldsymbol{dq}^{\mathbf{sgn}(n)n}} - \sum_{m\neq n}\left[T_{dq^{\mathrm{sgn}(n)n-\mathrm{sgn}(m)m}}\right]\bar{\mathbf{v}}^{*m}_{\boldsymbol{dq}^{\mathbf{sgn}(m)m}}\right\} \quad (14)$$

Since (11) can be re-written in the form of (14), it is proven that the MHDC of [19], [20] and the improved MHDC proposed in this paper can achieve an exact equivalent response in terms of estimating the voltage vector of the fundamental voltage component. Furthermore, simulation results of Fig. 4, verify that under several Harmonic Conditions (HC), where HC1, HC2 and HC3 are defined in Table II, both the MHDC of [19], [20] and the improved MHDC present an exact equivalent response on the accurate estimation of the $\mathbf{v}^{*\mathbf{1}}_{\boldsymbol{dq}^{\mathbf{+1}}}$. Although the two decoupling networks present an equivalent response, the improved MHDC proposed in this paper requires significantly less processing time compared to the MHDC of [19], [20], as it is analyzed below.

For a fair complexity analysis, both decoupling networks need to be designed for N=7, to consider the fundamental component (n=1) and the effect of the six most significant harmonic components (n=3, 5, 7, 9, 11, 13). Therefore, the process of the MHDC of [19], [20] for N=7 requires the repeated processing of (14) for seven times. As a consequence, in each control step the decoupling network should process N multi-subtractions $\left(\mathbf{v}_{\boldsymbol{dq}^{\mathbf{sgn}(n)n}} - \sum_{m\neq n}\bar{\mathbf{v}}^{*m}_{\boldsymbol{dq}^{\mathbf{sgn}(m)m}}\right)$, N^2 transformation matrices $\left[T_{dq^{\mathrm{sgn}(n)n}}\right]$, and N low-pass filtering matrices $[F(s)]$. In the case of the improved MHDC, for N=7, (11) must be repeated for seven times as well. At each control step the improved MHDC should process N multi-subtractions $\left(\mathbf{v}_{\boldsymbol{\alpha\beta}} - \sum_{m\neq n}\bar{\mathbf{v}}^{*m}_{\boldsymbol{\alpha\beta}}\right)$, $2N$ transformation matrices, and N low-pass filtering matrices $[F(s)]$. It is obvious that the proposed improved MHDC requires the processing of $2N$=14 transformation matrices instead N^2=49 matrices of the MHDC of [19], [20]. The complexity comparison is summarized in Table III. A further complexity analysis is also presented in Table III, where the two decoupling networks have been analyzed in terms of the required additions, subtractions and multiplications at each control step. It is obvious that the re-formulation of the decoupling cell according to the proposed improved MHDC (Section II.B) can significantly decrease the required processing time of the synchronization algorithm. The decreased complexity of the new improved MHDC is particularly useful, since the real-time operation of the inverter is enabled and a higher sampling rate can be adapted by the

TABLE III. Complexity Comparison of the Decoupling Networks

Decoupling Network	Complexity analysis in each control loop			
	Multi-subtractions	$\left[T_{dq^{\mathrm{sgn}(n)n}}\right]$	$[F(s)]$	Total mathematical operations
MHDC of [19] (N=7)	N	N^2	N	322 Multiplications 63 Additions 133 Subtractions
Improved MHDC (N=7)	N	N^2	N	112 Multiplications 28 Additions 98 Subtractions

TABLE IV. PERFORMANCE COMPARISON OF TWO PLLS

PLL algorithm	Required Processing Time (%)	Dynamic Response under grid faults	Accurate Resposne under		
			Voltage sag/phase shift	Frequency jump ($f \neq 50$ Hz)	Harmonic distortion
MHDC-PLL	100%	Fast	+	-	+
Freq. Adapt. MHDC-PLL	39%	Fast	+	+	+

inverter controller for an improved performance.

Further, an in-depth experimental complexity analysis has been performed, based on a widely used microcontroller, such as the Texas Instrument TMS320F28335 digital signal processor. The investigation demonstrates a significant improvement with regards to the algorithm complexity, since the process of the frequency adaptive MHDC-PLL at each control loop requires 54.6 μs instead of 140 μs in the case of the initial MHDC-PLL of [19], [20]. Therefore, the proposed synchronization method requires 61% less processing time compared to the initial MHDC-PLL, as summarized in Table IV. It is important to mention that an inverter controller based on the frequency adaptive MHDC-PLL can achieve a sampling rate of 8 kHz on TMS320F28335 (54.6 μs for the synchronization and 63 μs for the rest units of the inverter controller). On the other hand, if the inverter controller is based on the initial MHDC-PLL of [19], [20] the sampling rate should be decreased to 4 kHz on TMS320F28335 (140 μs for the synchronization and 63 μs for the rest of the units of the inverter controller). It is to be noted that the reduction on sampling rate of the controller can negatively affect the accuracy and the performance of the inverter.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The performance of the proposed frequency adaptive MHDC-PLL has been tested through simulation and experimental results in order to demonstrate the outstanding response of the new synchronization method. The investigation based simulations have been performed in MATLAB/Simulink. The experimental setup is based on a TMS320F28335 microcontroller (where the inverter controller has been applied), a Semikron SEMITeach (B6CI) inverter, a California Instrument 2253IX AC power source for emulating the grid, and an Elektro-Automatik EA-PSI 9750-20 DC power supply for emulating the DC bus of a PV system. It is worth mentioning that in both simulation and experimental studies, an 8 kHz sampling rate has been used for the inverter controller.

Simulations performed in MATLAB/Simulink show the synchronization response of the proposed frequency adaptive MHDC-PLL, as demonstrated in Fig. 5. The results of Fig. 5 show the synchronization response of the frequency adaptive MHDC-PLL and the MHDC-PLL of [19], [20] under the worst-case harmonic distortion (HC3 of Table II) at 0.3 s, a 10^o phase jump at 0.4 s, a 25% voltage sag at 0.5 s and -1.5 Hz frequency change at 0.6 s. The performance comparison of Fig. 5 between the two PLLs, proves that the frequency adaptive implementation of the QSG (Section II.A) enables the accurate synchronization under non-nominal frequencies ($0.6<t<0.75$ s). Therefore, the frequency adaptive MHDC-PLL not only requires a significantly less processing time as shown in Section III, but additionally, it can also achieve a superior performance under any grid conditions, as summarized in Table IV. From Fig. 5, it is obvious that the new frequency adaptive MHDC-PLL presents a very accurate response (even under the worst-case harmonic distortion for $t>0.3$ s) and a

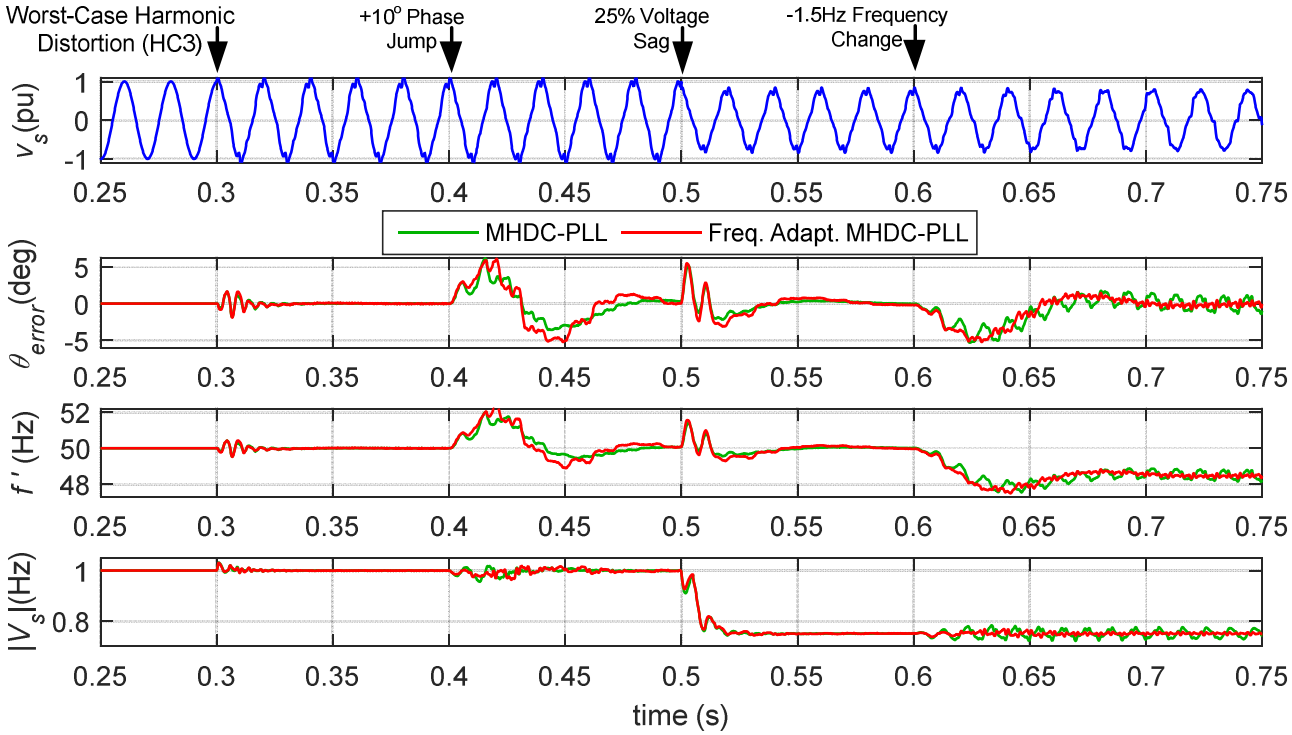

Fig. 5. Simulation results for the response of the frequency adaptive MHDC-PLL (new) and the MHDC-PLL under harmonic distortion, phase jump, voltage sag and frequency change events.

very fast synchronization under any grid disturbance (e.g., phase jump, voltage sag, frequency change).

The superior synchronization performance of the proposed frequency adaptive MHDC-PLL has also been experimentally verified as shown in Fig. 6. The experimental results of Fig. 6(a) demonstrate the response of the new synchronization method when the worst-case harmonic distortion (HC3 of Table II) occurs at the grid voltage. The experiments show that the proposed PLL can decouple the effect of harmonics within 10 ms. The initial voltage in Fig. 6(b)-(d) has harmonic distortion with the worst-case harmonics (HC3) and then a grid disturbance is applied. According to Fig. 6(b), a fast and accurate synchronization is achieved under a 25% voltage sag, which can enable a proper FRT operation of the grid tied inverter. Fig. 6(c) demonstrates the operation of the new PLL under a 1 Hz frequency change. It is worth mentioning that the frequency adaptive MHDC-PLL presents a very accurate response under non-nominal frequencies due to the adaptive QSG. Finally, the fast and accurate synchronization response under a 10^o phase jump is demonstrated in Fig. 6(d). According to the experiments of Fig. 6, the proposed frequency adaptive MHDC-PLL can achieve a fast and accurate synchronization under any grid conditions. Such an advanced PLL based synchronization method can be an ideal solution for the synchronization of grid tied inverters.

The synchronization accuracy under harmonic distortion can be very beneficial for the power quality of the grid-tied inverter as discussed in [10] and [20], while the dynamic response of the synchronization, especially under voltage sags, can enable a proper FRT operation of the inverter in order to enhance the stability of the power system under grid faults. A simulation based investigation has been performed here to demonstrate the beneficial effect of a fast and accurate synchronization on the operation of the grid-tied inverter as shown in Fig. 7. For this investigation, an open loop PQ controller designed in the *dq*-frame [24] is used to generate the reference currents $\mathbf{I}^*_{\boldsymbol{dq}} = [I_d^*\ I_q^*]^*$. Then, a current controller based on a PI controller and also designed in the *dq*-frame [24], [25] is used to regulate the inverter current. It is to be noted that the current controller is enhanced with a harmonic compensation module [25] in order to minimize the distortion of the injected current. Further, the PQ controller is enhanced with FRT capabilities [26] in order to provide a proper voltage support under voltage sags, in terms of proper reactive current injection I_Q, according to $I_Q=k(v_N-v_s)$, where k is set to 2 for the purposes of this investigation and v_N is the nominal grid voltage [26].

Therefore, the simulation results of Fig. 7 present the inverter operation when a) a SOGI-PLL (t<0.5 s) and b) when the proposed Frequency Adaptive MHDC-PLL (t>0.5s) are used for the grid synchronization of the inverter. It should be noted that the SOGI-PLL does not present immunity against harmonic distortion in contrast with the new PLL which presents a great robustness against harmonics. The inverter operation is demonstrated under highly harmonic distorted grid voltage (HC2 of Table II) and under a 25% voltage sag. It is obvious that the accuracy of the new synchronization against harmonics enables the accurate generation of reference currents

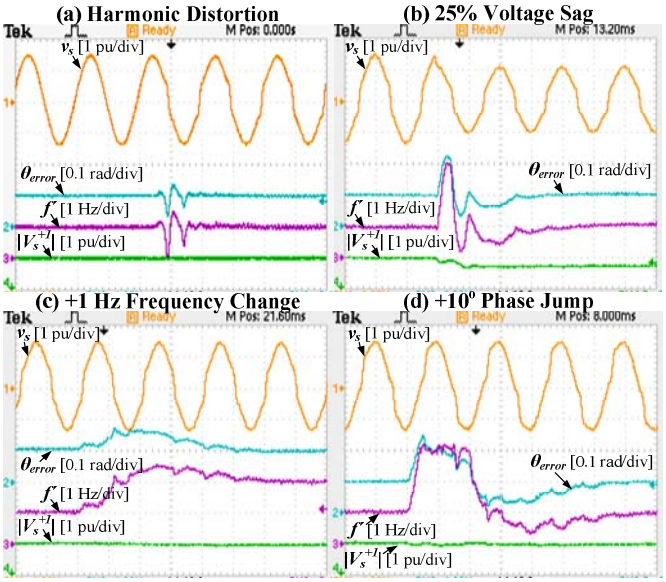

Fig. 6. Experimental results for the synchronization response of the frequency adaptive MHDC-PLL under: (a) a harmonic distorted voltage, (b) a 25% voltage sag, (c) an 1 Hz frequency change, and (d) a 10^o phase jump. The time division of the results is 10 ms/div.

($\mathbf{I}^*_{\boldsymbol{dq}}$) while the inaccuracies of SOGI-PLL cause undesired oscillations on the reference currents. The oscillations on the reference currents cause an increased total harmonic distortion of the current (THD_i) in the case of the SOGI-PLL, with a THD_i=2.15% when there is no voltage sag and THD_i=4.5% when a voltage sag occurs. On the other hand, the accuracy of the proposed frequency adaptive MHDC-PLL enables an oscillation-free generation of the reference currents and thus, a high quality current injection is achieved, with a THD_i=1.5% under normal operation and voltage sag. Further, the dynamic response of the frequency adaptive MHDC-PLL enables a fast and a proper FRT operation of the inverter, where a reactive power support is properly injected into the grid within 15 ms, for enhancing the stability of the power system. During the FRT operation the injected active power is decreased to maintain the injected current within the inverter limits. Hence, the results of Fig. 7 demonstrate that the accurate and fast response of the frequency adaptive MHDC-PLL is particularly beneficial for the operation of the grid tied inverter, in terms of increasing the power quality and of enabling an appropriate dynamic and FRT operation of the inverter.

V. CONCLUSION

In this paper, two new methods have been proposed: one for decreasing the complexity of the MHDC-PLL and one for enhancing its performance against non-nominal grid frequencies. Hence, the proposed frequency adaptive MHDC-PLL requires a significantly less processing time and presents a superior performance in contrast to the original one. Thus, the proposed frequency adaptive MHDC-PLL can achieve a fast and accurate response under any grid disturbances and under highly harmonic distorted voltage. As a consequence, the proposed synchronization method can be beneficial for the operation of a grid-tied inverter in terms of power quality and also of dynamic performance.

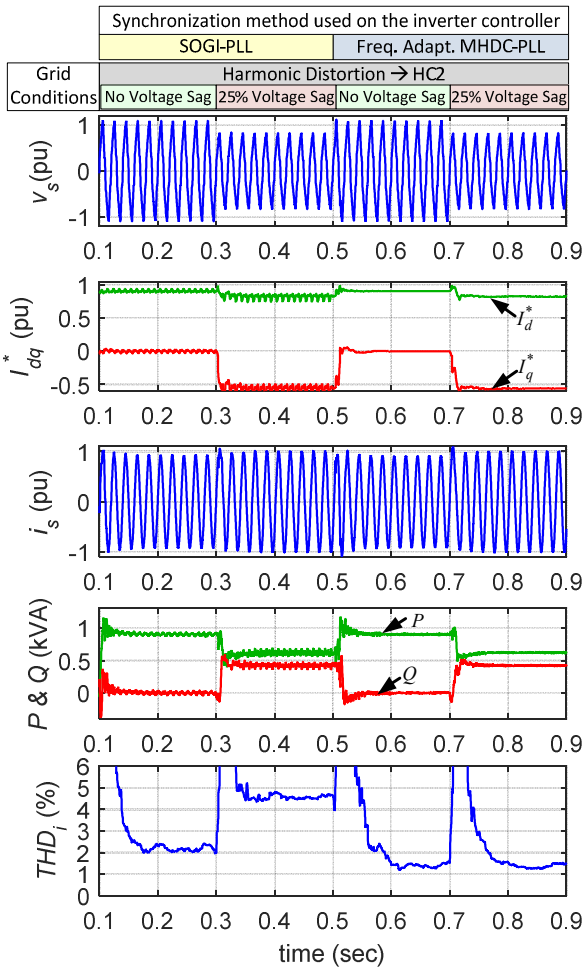

Fig. 7. Simulation results for the inverter operation when (a) a SOGI-PLL and (b) a frequency adaptive MHDC-PLL is used for the synchronziation of the inverter under harmonic distorted voltage and a voltage sag event.

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