A Robust Synchronization to Enhance the Power Quality of Renewable Energy Systems

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***Abstract*—The increasing penetration of renewable energy sources in the power grid requires high quality power injection under various grid conditions. The synchronization method, usually a phase-locked loop (PLL) algorithm, is directly affecting the response of the grid side converter of the renewable energy source. This paper proposes a new PLL algorithm that uses an advanced decoupling network implemented in the stationary reference frame with limited requirements for processing time to enable a fast and accurate synchronization even under harmonic distorted voltage and low-voltage grid faults. The robust response of the proposed PLL is validated and the effect of the proposed synchronization on the performance of the grid-connected renewable energy system is investigated. This investigation proves that the robust, accurate and dynamic response of the new PLL can enhance the quality of the injected power from the renewable energy source and can also enable an appropriate fault ride through operation under harmonic distorted voltage and grid faults.**

***Index Terms*—Harmonic distortion, phase locked loop, power quality, renewable energy, synchronization, unbalanced faults.**

I. Introduction

RENEWABLE Energy Sources (RES) connected to the power grid have now reached significant penetration levels and can affect the power quality and the grid stability of the power system. Therefore, there is a need to advance the controllers for the Grid Side power electronic Converter (GSC) of RES to meet the modern grid codes [1]-[4]. According to these regulations, the GSC of a RES needs to enable a high quality current injection under normal and harmonic distorted grid voltage. Moreover, the RES controller must be equipped with Fault Ride Through (FRT) capability to enhance the power system stability by participating in the support of the power system under grid faults.

The controller of the GSC [5]-[8] is based on the synchronization unit, the active and reactive power (PQ) controller and the current controller, as shown in Fig. 1. The synchronization unit usually consists of a phase locked loop (PLL) algorithm to detect the phase and amplitude of the grid voltage at the point of common coupling (PCC). The PQ controller is responsible for generating the reference currents under normal and faulty grid conditions and the current controller ensures a proper current injection. The PQ and current controllers are directly affected by the response of the synchronization method and therefore, the PLL performance is critical for an appropriate operation of grid-connected RES.

The synchronization method is normally a PLL algorithm when the controller of the GSC is designed on the synchronous rotating reference frame with Proportional-Integral (PI) controllers [5]-[8]. Conventional PLL algorithms [9]-[10] are simplified in structure and can provide proper operation only under normal and balanced grid voltage. These PLLs are inaccurate under abnormal grid conditions, since they are sensitive to the oscillations of the synchronization signals caused by the existence of the negative sequence voltage (unbalanced conditions) and the low-order voltage harmonic distortion. These inaccuracies can affect the power quality of the RES. The PLL in [11] adjust the tuning parameters to reduce the bandwidth of the synchronization and to minimize the inaccuracies, but the dynamic operation of the PLL is unavoidably affected. Some other PLLs [12]-[14] are enhanced with adaptive or notch filtering techniques to cancel out these oscillations. However, these filters can also decelerate the synchronization response, which affects the dynamic FRT operation of the RES. The modified PLL in [15] is based on a non-linear adaptive approximation technique and presents higher degree of immunity to noise. Unfortunately, this PLL presents very slow dynamics and thus, it is not to be used in control paths, as mentioned in [15]. A three-phase enhanced PLL (3E-PLL) presented in [16] is based on four single-phase E-PLL and on symmetrical components. The performance of 3E-PLL is compared with other PLLs in [17]. The 3E-PLL is accurate under unbalanced grid conditions, can relatively mitigate, but not eliminate, the effect of the harmonic distortion on the synchronization accuracy and presents slower dynamics compared to the PLLs presented in [18]-[20].

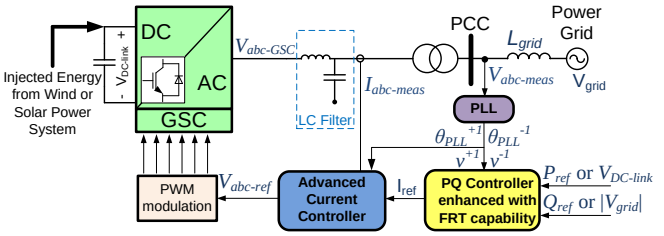

Fig. 1. The structure of a GSC control enhanced with fault ride through capability when the synchronization is achieved by the proposed PLL.

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Some interesting techniques designed in double reference frame [18]-[20], [21, Ch. 8], are using a decoupling network to cancel out dynamically the double frequency oscillation of the positive sequence of the grid voltage due to the unbalanced voltage. These PLLs achieve a fast and accurate synchronization under balanced or unbalanced low-voltage grid faults and enable the FRT operation of RES. However, they are sensitive to voltage harmonic distortion.

Moving Average Filters (MAF) based PLLs [22]-[24] have a simplified structure and are robust against unbalanced and harmonic distorted grid conditions. The discrete implementation of such techniques based on MAF causes some small inaccuracies when the grid frequency deviates from the nominal value. These inaccuracies can be minimized, but not eliminated, by adjusting the number of samples according to the operating frequency [22]. The only way to completely eliminate these inaccuracies is to use a variable sampling period for the PLL to adapt the window length of the MAF [25], but the variable sampling rate can cause restrictions on the GSC controller. Nevertheless, even if these inaccuracies are overcome, the main disadvantage of the MAF based PLLs is the slow dynamic performance of these PLLs. An interesting synchronization solution is proposed in [17], which is based on variable sampling period and on a sliding Goertzel transform filter. This technique shows improved dynamics and immunity to the voltage disturbances, however the variable sampling rate on the PLL may not be always possible due to the restrictions of the GSC controller.

Another synchronization solution is the Frequency Locked Loop (FLL). Some robust FLL methods are presented in [26]-[27], but unfortunately, the synchronization through FLL is only appropriate in the unusual case where the control of the GSC is designed on the stationary reference frame (αβ-frame).

Thus, there is a need for new synchronization methods, which should be accurate under distorted voltage and abnormal grid conditions without affecting the dynamic response of the PLL. This paper proposes a new PLL algorithm that uses a novel Decoupling Network designed in the αβ-frame (DNαβ-PLL) that can achieve a dynamic and accurate synchronization under harmonic distorted and unbalanced grid voltage. The proposed decoupling network cancels out dynamically the oscillations of the positive sequence of the grid voltage due to the unbalanced and harmonic distorted grid voltage. The new DNαβ-PLL is the evolution of the recently proposed in [28] Multi-Sequence/Harmonic Decoupling Cell PLL (MSHDC-PLL). The two PLLs can achieve the same fast and accurate synchronization response under any grid conditions but the proposed DNαβ-PLL requires 76% less processing-time than the MSHDC-PLL. The decoupling network of the proposed PLL is formulated and designed in the αβ-frame instead of in each synchronous reference frame, which requires significantly less Park's transformations for processing the algorithm. Thus, the complexity of the algorithm is minimized; this is a critical aspect for controlling real-time power electronic applications. The outstanding performance of the proposed PLL is proven through simulation and experimental results. Furthermore, this paper investigates how the new PLL is beneficially affecting the RES performance in terms of enhancing the power quality of the injected energy and of enabling the proper FRT operation of the RES. Thus, the proposed PLL is a recommended solution for the synchronization of RES under low voltage grid faults and harmonic distorted environments.

The new PLL algorithm is proposed in Section II and an enhanced GSC control is presented in section III. Section IV contains simulation and experimental results to validate the synchronization response and to prove the beneficial effect on the RES performance under any grid conditions.

II. The New DNαβ-PLL

The synchronization unit in grid-connected RES is responsible to detect accurately and fast the voltage amplitude and phase angle of the positive sequence of the grid voltage at the PCC. Under normal grid operation conditions, conventional PLLs [9]-[10] can achieve accurate response by using Park's transformation to express the grid voltage to the synchronous rotating frame (dq_{+1}-frame), rotating with the synchronous speed of the positive sequence of the voltage, or to the stationary frame ($\alpha\beta$-frame). Unfortunately, the performance of the conventional synchronization methods is inaccurate under abnormal grid conditions due to the coupling effect between the existing voltage sequences and harmonics. This paper proposes a new PLL, enhanced with an innovative decoupling network design in the $\alpha\beta$-frame (DNαβ), to enable the accurate and robust synchronization.

A. Design Guidelines

In case of harmonic distorted and unbalanced grid, the voltage can be analyzed as a sum of the existing rotating voltage vectors, each one rotating with a different speed. Thus, the grid voltage is a sum of positive (+1) and negative (-1) sequences and the existing significant low-order harmonics (h_1,...,h_k) and can be expressed in the αβ-frame by,

$$\begin{aligned} \boldsymbol{v}_{\alpha\beta} &= \left[T_{\alpha\beta}\right]\boldsymbol{v}_{abc} = \boldsymbol{v}_{\alpha\beta}^{+1} + \boldsymbol{v}_{\alpha\beta}^{-1} + \boldsymbol{v}_{\alpha\beta}^{h_1} + \cdots + \boldsymbol{v}_{\alpha\beta}^{h_k} \\ \Leftrightarrow \boldsymbol{v}_{\alpha\beta} &= \sum_{n=1,-1,h_1,..,h_k} V^n \begin{bmatrix} \cos(n\omega t + \theta^n) \\ \sin(n\omega t + \theta^n) \end{bmatrix} \end{aligned} \quad (1)$$

$$\text{where } \left[T_{\alpha\beta}\right] = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta - 120^o) & \cos(\theta + 120^o) \\ -\sin(\theta) & -\sin(\theta - 120^o) & -\sin(\theta + 120^o) \end{bmatrix}. \quad (2)$$

The voltage vector can equivalently be expressed in any dq_n-frame as

$$\boldsymbol{v}_{\boldsymbol{dq_n}} = \left[T_{dq^n}\right]\left(\left[T_{\alpha\beta}\right]\boldsymbol{v}_{\boldsymbol{abc}}\right) = \begin{bmatrix} v_{d_n} \\ v_{q_n} \end{bmatrix} = \left[T_{dq^n}\right]\boldsymbol{v}_{\boldsymbol{\alpha\beta}} = \boldsymbol{v}_{\boldsymbol{dq_n}}^{\boldsymbol{n}} + \sum_{m\neq n} \boldsymbol{v}_{\boldsymbol{dq_n}}^{\boldsymbol{m}} \quad (3)$$

$$\text{where } \underbrace{\boldsymbol{v}_{\boldsymbol{dq_n}}^{\boldsymbol{n}} = V^n \begin{bmatrix} \cos(\theta^n) \\ \sin(\theta^n) \end{bmatrix}}_{\textit{Oscillation free term}}, \ \underbrace{\boldsymbol{v}_{\boldsymbol{dq_n}}^{\boldsymbol{m}} = V^m \left[T_{dq^{n-m}}\right] \begin{bmatrix} \cos(\theta^m) \\ \sin(\theta^m) \end{bmatrix}}_{\textit{Oscillation terms}} \quad (4)$$

and n and m can be any of the existing sequences or harmonic components (+1, -1, h_1, …, h_k). It is to be noted that a harmonic order H_1 under unbalanced grid conditions, requires

both h_1= +H_1 and h_2 = -H_1 to be fully described (where H_1 can be equal to -5, +7, -11, +13), similarly to how an unbalanced fundamental component (1) requires both positive (+1) and negative (-1) sequence to be analyzed in detail under unbalanced faults. The transformation from dq_m- to dq_n-frame is achieved by,

$$\left[T_{dq^{n-m}}\right]=\left[T_{dq^{m-n}}\right]^{T}=\begin{bmatrix}\cos(n-m)\omega t & \sin(n-m)\omega t\\ -\sin(n-m)\omega t & \cos(n-m)\omega t\end{bmatrix}. \quad (5)$$

As shown in (3), an abnormal grid voltage vector expressed in the dq_n -frame consists of an oscillation free term $\boldsymbol{v}^{n}_{dq_n}$, and the sum of the oscillation-terms $\boldsymbol{v}^{m}_{dq_n}$. The $\boldsymbol{v}^{n}_{dq_n}$ is an oscillation free signal and it consists of the voltage vector v^n (rotating with $n\cdot\omega$ speed) expressed in the corresponding dq_n -frame rotating also with $n\cdot\omega$. Accordingly, the $\boldsymbol{v}^{m}_{dq_n}$ are signals with $(n\text{-}m)\cdot\omega$ oscillations, since the existing vectors $\boldsymbol{v}^{m}$ (rotating with $m\cdot\omega$ speed) are expressed in the dq_n-frame rotating with $n\cdot\omega$. The oscillation terms $\boldsymbol{v}^{m}_{dq_n}$ can cause the inaccuracies on the conventional synchronization methods.

A new decoupling network is proposed that allows an accurate detection of each voltage component $\boldsymbol{v}^{n}$, by dynamically cancelling-out the oscillations that are created due to the coupling between the voltage components. The oscillations-free terms $\boldsymbol{v}^{n}_{dq_n}$ for each sequence or harmonic voltage can be calculated by,

$$\boldsymbol{v}^{\boldsymbol{n}}_{\boldsymbol{dq_n}}=\left[T_{dq^{n}}\right]\boldsymbol{v}^{\boldsymbol{n}}_{\boldsymbol{\alpha\beta}}=\left[T_{dq^{n}}\right]\left(\boldsymbol{v}_{\boldsymbol{\alpha\beta}}-\sum_{m\neq n}\boldsymbol{v}^{\boldsymbol{m}}_{\boldsymbol{\alpha\beta}}\right). \quad (6)$$

However, since the vectors $\boldsymbol{v}^{m}_{\alpha\beta}$ can not be accurately calculated due to the coupling effects, it is suggested to replace these vectors with the filtered estimated vectors $\bar{\boldsymbol{v}}^{*m}_{\alpha\beta}$ in order to determine the estimation vectors $\boldsymbol{v}^{*n}_{\alpha\beta}$ and $\boldsymbol{v}^{*n}_{dq_n}$ by,

$$\boldsymbol{v}^{*\boldsymbol{n}}_{\boldsymbol{dq_n}}=\left[T_{dq^{n}}\right]\boldsymbol{v}^{*\boldsymbol{n}}_{\boldsymbol{\alpha\beta}}=\left[T_{dq^{n}}\right]\left(\boldsymbol{v}_{\boldsymbol{\alpha\beta}}-\sum_{m\neq n}\bar{\boldsymbol{v}}^{*\boldsymbol{m}}_{\boldsymbol{\alpha\beta}}\right). \quad (7)$$

The estimation vectors require a low-pass filtering with a cut-off frequency (ω_f) of $2\pi\cdot 50/\sqrt{2}$ rad/s, to eliminate any remaining oscillations on the estimated voltage vectors [18]-[20], [28]. Since each vector is rotating with different $n\cdot\omega$ speed, it is necessary that the filtering should be performed in the corresponding dq_n -frame for each vector, in order to achieve an equivalent filtering on the voltage components. Thus, the estimated vectors $\boldsymbol{v}^{*n}_{\alpha\beta}$ must first be transformed to $\boldsymbol{v}^{*n}_{dq_n}$ and then be filtered to $\bar{\boldsymbol{v}}^{*n}_{dq_n}$, as shown below,

$$\begin{aligned}&\boldsymbol{v}^{*\boldsymbol{n}}_{\boldsymbol{dq_n}}=\left[F(s)\right]\boldsymbol{v}^{*\boldsymbol{n}}_{\boldsymbol{dq_n}} \text{ and } \bar{\boldsymbol{v}}^{*\boldsymbol{n}}_{\boldsymbol{\alpha\beta}}=\left[T_{dq^{-n}}\right]\bar{\boldsymbol{v}}^{*\boldsymbol{n}}_{\boldsymbol{dq_n}}\\ \Leftrightarrow\ &\bar{\boldsymbol{v}}^{*\boldsymbol{n}}_{\boldsymbol{\alpha\beta}}=\left[T_{dq^{-n}}\right]\left[F(s)\right]\boldsymbol{v}^{*\boldsymbol{n}}_{\boldsymbol{dq_n}}=\left[T_{dq^{-n}}\right]\left[F(s)\right]\left[T_{dq^{n}}\right]\boldsymbol{v}^{*\boldsymbol{n}}_{\boldsymbol{\alpha\beta}}\end{aligned} \quad (8)$$

where

$$\left[F(s)\right]=\frac{\omega_f}{s+\omega_f}\left[I\right]. \quad (9)$$

The results presented in (8) can be replaced in (7) to enable the estimation of each voltage vector, thus obtaining,

$$\boldsymbol{v}^{*\boldsymbol{n}}_{\boldsymbol{dq_n}}=\left[T_{dq^{n}}\right]\boldsymbol{v}^{*\boldsymbol{n}}_{\boldsymbol{\alpha\beta}}=\left[T_{dq^{n}}\right]\left(\boldsymbol{v}_{\boldsymbol{\alpha\beta}}-\sum_{m\neq n}\left[T_{dq^{-n}}\right]\left[F(s)\right]\left[T_{dq^{n}}\right]\boldsymbol{v}^{*\boldsymbol{m}}_{\boldsymbol{\alpha\beta}}\right). \quad (10)$$

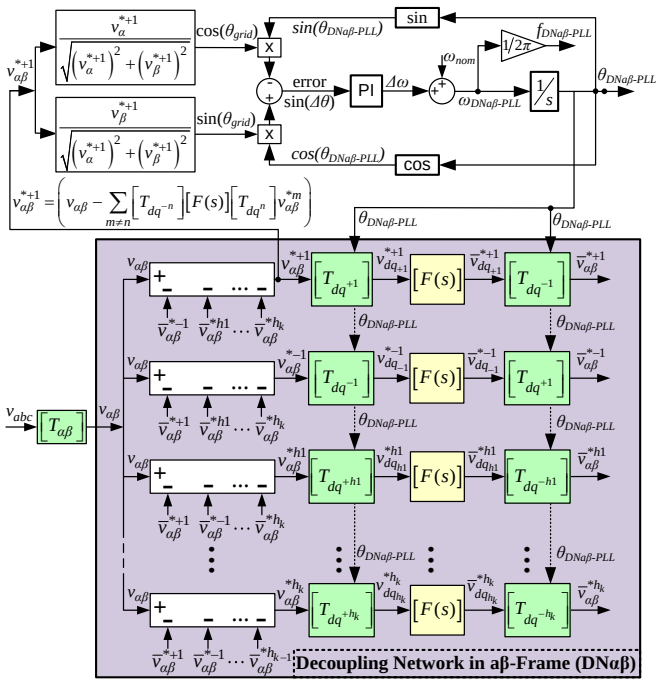


Fig. 2. Block diagram of the new DNαβ-PLL.

Hence, the proposed decoupling network (DNαβ) is based on the multiple use of (10) for n=+1, -1, h_1,..., h_k for estimating each oscillation free voltage components $\boldsymbol{v}^{*n}_{dq_n}$ as shown in the block diagram in Fig. 2. The block diagram illustrates that the proposed DNαβ is a cross feedback network with recursive filtering characteristics that allow fast, dynamic and accurate decoupling of the grid voltage.

The proposed DNαβ enables a proper decoupling between the existing voltage vector components and therefore, can dynamically and accurately estimate the value of each voltage component ($\boldsymbol{v}^{*n}_{\alpha\beta}$ and $\boldsymbol{v}^{*n}_{dq_n}$). The proposed PLL can be implemented by using the pure positive sequence voltage component ($\boldsymbol{v}^{*+1}_{\alpha\beta}$), estimated by the DNαβ, as an input to the conventional PLL algorithm of [10], designed in αβ-frame. Therefore, the proposed DNαβ-PLL can achieve a fast and accurate detection of the phase angle of the positive sequence of the voltage. The PLL algorithm is based on controlling the $\Delta\theta$ of (11) to track zero through a PI controller and so the detected angle ($\theta_{DN\alpha\beta\text{-}PLL}$) tracks the grid phase angle (θ_{grid}).

$$\begin{aligned}&\Delta\theta=\theta_{grid}-\theta_{DN\alpha\beta-PLL}\approx\sin(\theta_{grid}-\theta_{DN\alpha\beta-PLL})\\ \Leftrightarrow\ &\Delta\theta\approx\sin(\theta_{grid})\cos(\theta_{DN\alpha\beta-PLL})-\sin(\theta_{DN\alpha\beta-PLL})\cos(\theta_{grid})\end{aligned} \quad (11)$$

Another important aspect is the optimal tuning of the new PLL, which can be achieved according to the linearized small signal model analysis of [19]-[20], [21, Ch. 4]. In case where the transfer function of the PI controller of the PLL is given by k_p+1/($T_i s$), the transfer function of the synchronization unit can be simplified to a second-order transfer function, as shown in (12). The transfer function of the PLL presents a low-pass filtering characteristic, which is crucial in order to cancel out the high-order harmonics and the noise of the grid voltage.

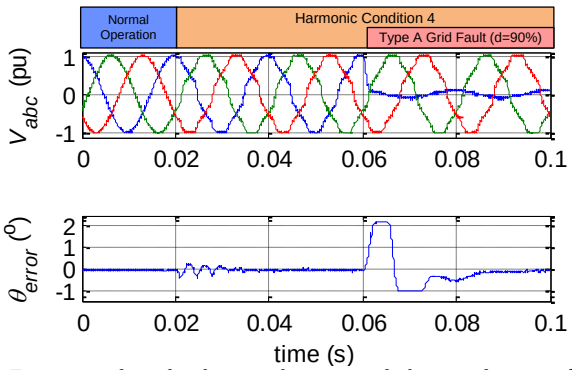


Fig. 3. Experimental results showing the estimated phase angle error of the DNαβ-PLL (implemented for N=10) under the worst case harmonic distortion (HC-4) and an unbalanced grid fault.

$$\frac{\theta_{DN\alpha\beta-PLL}}{\theta_{grid}} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{k_p \cdot s + 1/T_i}{s^2 + k_p \cdot s + 1/T_i} \quad (12)$$

The tuning parameters k_p and T_i can be calculated according to (13), where ζ should be set to $1/\sqrt{2}$ for an optimally damped PLL response and the Settling Time (T_s) defines the dynamic response of the proposed PLL.

$$k_p = \frac{9.2}{T_s} \quad and \quad T_i = 0.047 \cdot \zeta^2 \cdot T_s^2 \quad (13)$$

For the purpose of this paper the tuning parameters are set to k_p=12.35 and T_i=0.013, to achieve the faster possible response of the PLL without violating the frequency operation window (from 47.5 Hz to 51.5 Hz) of the German grid codes [2] even for the worst-case low-voltage fault according to [19]. A faster tuning configuration can lead to high frequency overshoot under a grid fault, which can cause an undesired disconnection of the RES from the grid. Notwithstanding, the proposed DNαβ-PLL can also be tuned to a faster or slower response depending on the purpose of the application.

Another critical aspect for the design of the PLL is to define which harmonics (n) are to be cancelled-out by the proposed DNαβ under general grid conditions. It is obvious that the accuracy of the PLL depends on the number of sequences and harmonics (N) eliminated by the decoupling network. Since an infinite number of harmonics is impossible to be considered due to complexity issues, the decoupling network should focus on eliminating the negative sequence and the most significant low-order pairs of harmonics. The rest of the harmonics can be ignored, since their effect is minimized due to the low-pass filtering characteristics of the DNαβ as mentioned in Section II.B. An investigation has been performed for the accuracy of the proposed PLL for different number of harmonics (N) considered by the DNαβ. The accuracy of the PLL has been studied according to the maximum harmonic distortion of the grid voltage as defined by the EN50160 standard. This set of harmonics is defined as harmonic conditions 4 (HC-4) and is analytically presented in Table IV. The investigation shows that when the DNαβ is designed with N=10 to eliminate the negative sequence and the pairs of harmonics up to order thirteen (n = ±1, ±5, ±7, ±11, ±13) the proposed PLL can achieve an accurate response. The new PLL has been implemented in a TMS320F28335 digital signal processor (DSP). The experimental results of Fig. 3 present the response of the DNαβ-PLL (with N=10) under the worst-case harmonic distortion (HC-4) and under an unbalanced grid fault (Type B with 90% voltage sag (d)). The estimated phase angle error of the proposed PLL, presented in Fig. 3, is less than 0.05 degrees (θ_{error}<0.05°) due to the effect of the harmonics not considered in the decoupling network. Thus, for an accurate PLL response and an adequate algorithm complexity, the DNαβ-PLL should be designed for N=10 to consider the harmonics up to order thirteen.

B. *Complexity Assessment*

An assessment of the complexity of the PLL algorithm is essential for real-time practical applications. For the purpose of this experimental benchmarking investigation, a 32-bit TMS320F28335 DSP of Texas Instruments has been used, since it is a conventional and widely used microcontroller for controlling such power electronics applications. The complexity of several PLL algorithms, including the proposed one, has been assessed based on the required processing time of each algorithm to be executed in the TMS320F28335 DSP.

The recursive filter of the proposed DNαβ enables a dynamic decoupling of the voltage without affecting the time response of the DNαβ-PLL. The detailed analysis of the recursive filtering character of the proposed decoupling network is considered the same as the one presented in [28], since the DNαβ and MSHDC present identical transfer functions. The DNαβ and MSHDC [28] present an equivalent response; however, the decoupling in DNαβ is always performed in the $\alpha\beta$-frame in contrast with the MSHDC, where the decoupling is performed in each dq_n-frame. The

TABLE I
COMPLEXITY COMPARISON BETWEEN THE DNab AND THE MSHDC

Decoupling Network	Complexity analysis in each control loop			
	$\left(v_{dq_n} - \sum_{m\neq n} \bar{v}_{dq_n}^{*m}\right)$ or $\left(v_{\alpha\beta} - \sum_{m\neq n} \bar{v}_{\alpha\beta}^{*m}\right)$	$[T_{dq}{}^n]$	$[F(s)]$	**Total**
MSHDC (N=10)	N	N^2	N	640 Multiplications 120 Additions 280 Subtractions
DNαβ (N=10)	N	$2N$	N	160 Multiplications 40 Additions 200 Subtractions

Notes:
- **Each** $\left(v_{\alpha\beta} - \sum_{m\neq n} \bar{v}_{\alpha\beta}^{*m}\right)$ **or** $\left(v_{dq_n} - \sum_{m\neq n} \bar{v}_{dq_n}^{*m}\right)$ → requires 2·(N-1) Subtractions
- **Each** $[T_{dq}]$ → requires 6 Multiplications + 1 Addition + 1 Subtractions
- **Each** $[F(s)]$ → requires 4 Multiplications + 2 Additions

TABLE II
RESPONSE AND PROCESSING TIME OF SEVEN DIFFERENT PLLS

PLL algorithm	Required Processing Time (μs)	Dynamic Response under grid faults	Accurate Response under			
			Balanced voltage	Unbalanced voltage	Harmonic distortion	$f \neq$ nominal
dq-PLL	7.9	Fast	+	-	-	+
ddsrf-PLL	15.2	Fast	+	+	-	+
dαβ-PLL	17.3	Fast	+	+	-	+
MAF-PLL	8.5	Slow	+	+	+	-
mod. MRF-PLL	16.0	Slow	+	+	+	-
MSHDC-PLL	258.2	Fast	+	+	+	+
DNαβ-PLL	**63.7**	**Fast**	+	+	+	+

(a)

(b)

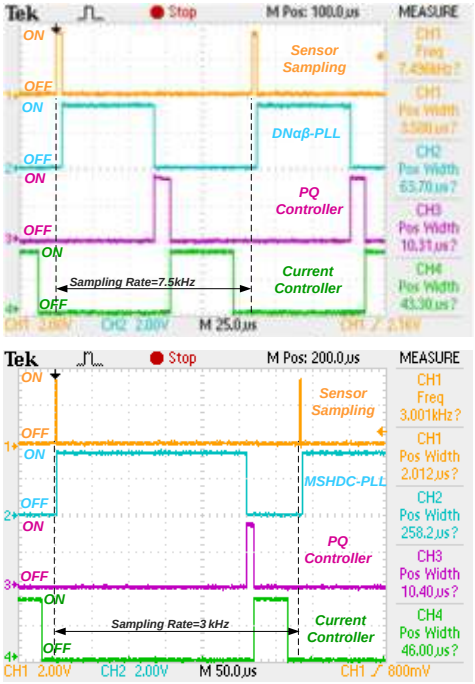


Fig. 4. Required processing time for each unit of the GSC controller in TMS320F28335 DSP: (a) when the proposed DNαβ-PLL is used (t_{div}=25µs/div), and (b) when the MSHDC-PLL is used (t_{div}=50µs/div). To be noted that when the signal is ON the corresponding algorithm is executed.

complete decoupling of a voltage vector with N components (positive, negative sequence and N-2 harmonics) using the proposed DNαβ requires the process of N $(v_{\alpha\beta} - \Sigma_{m\neq n}\bar{v}^{*m}_{\alpha\beta})$ multi-subtractions, $2N$ $[T_{dq}{}^n]$ transformations, and N $[F(s)]$ low pass filters in each control loop. In comparison, in case of the MSHDC, the algorithm requires the execution of N $(v_{dq_n} - \Sigma_{m\neq n}\bar{v}^{*m}_{dq_n})$ multi-subtractions, N^2 $[T_{dq}{}^n]$ matrix transformations, and N $[F(s)]$ matrix low-pass filters in each control loop. The complexity comparison between the two decoupling networks is analytically presented in Table I. For the proper accuracy of both PLLs, harmonics up to order thirteen (N=10) should be eliminated by the decoupling network as already explained in Section II.A, since the effect of higher orders harmonics is minimized by the low pass filtering characteristic of the decoupling network [28]. Therefore, the proposed DNαβ requires only twenty transformations ($2N$) in comparison with one hundred transformations (N^2) required by the MSHDC. Since, the process of each transformation requires 2.4 µs in the TMS320F28335 DSP, the proposed PLL requires considerable less execution time than the MSHDC-PLL. More details about the complexity analysis of the two synchronization methods are presented in Table I, where the complexity of the two decoupling networks (for N=10) is analyzed in terms of the required operations (32-bit multiplications, 32-bit additions and 32-bit subtractions) in each control step. It is to be noted that the analysis in terms of the required operators has been verified according to the assembly code of the DSP. Hence, the proposed DNαβ achieves an equivalent with the MSHDC fast and accurate decoupling of the voltage and additionally, requires significantly less processing time, which is important in such real-time applications.

Table II presents the required processing time in µs, the accuracy and the dynamic response of seven different PLL algorithms, the dq-PLL [9], the ddsrf-PLL [18], the dαβ-PLL [19], the MAF-PLL [22]-[23], the modified MRF-PLL [22], [24], the MSHDC-PLL (for N=10) [28], and the proposed DNαβ-PLL (for N=10). It has to be noted that the dq-PLL is inaccurate for unbalanced or harmonic distorted voltages and that the ddsrf-PLL and the dαβ-PLL are fast but inaccurate under harmonic distorted voltages. The MAF-PLL and the modified MRF-PLL are accurate under unbalanced and harmonic distorted voltages, but they present slow dynamics and possible inaccuracies under non-nominal frequencies. The MSHDC-PLL and the new DNαβ-PLL present fast and accurate response under unbalanced, harmonic distorted voltages and under any grid frequency. Both PLLs have been designed for N=10, to consider the ±1, ±5, ±7, ±11, ±13 orders of sequences/harmonics. It is obvious that the proposed DNαβ-PLL presents the most outstanding performance, since it presents a fast and accurate response under any abnormal grid conditions and furthermore, requires 63.7 µs instead of 258.2 µs required by the corresponding MSHDC-PLL due to the significantly less required transformations.

Fig. 4 presents the required processing time of the main units of the GSC controller as shown in Fig. 1, when they are executed in a conventional microcontroller, such as the TMS320F28335 DSP of Texas Instruments. The results in Fig. 4(a) show that the new DNαβ-PLL requires a processing time of 63.7 µs (as already mentioned in Table II). The required processing time for the sensor sampling (3.5 µs), current controller (43.3 µs) and PQ controller (10.3 µs) are also presented in Fig. 4(a), where the GSC controller operates in real-time with a sampling rate of 7.5 kHz. The adequate complexity of the DNαβ-PLL (implemented with N=10) in comparison to the MSHDC-PLL, which presents the same dynamic and accurate performance, is one of the main contributions of this paper since it enables the real-time execution of the algorithm using proper sampling rates. Experimental results of Fig. 4(b) show that the MSHDC-PLL [28] requires an execution time of 258.2 µs in each control loop in the TMS320F28335 DSP. Thus, for a real-time execution of the GSC control method, the sampling rate has to be decreased from 7.5 kHz to 3 kHz as shown in Fig. 4, when the MSHDC-PLL is used. Such a reduction on the sampling rate of the GSC controller is undesired since low sampling rates can affect the accuracy and the performance of the GSC. Therefore, the proposed DNαβ-PLL can be straightforwardly applied to a real-time controller of RES and can enable a fast and accurate synchronization under abnormal grid conditions in order to enhance the power quality of the RES.

III. Enhanced GSC Control of a RES

Advanced GSC control strategies have to be designed to meet the modern grid requirements for interconnecting RES. According to Fig. 5, the GSC control is based on the PLL algorithm to ensure the grid synchronization, the PQ controller

to generate the reference currents under normal and FRT operation and the current controller to enable a proper and high quality current injection. It is seen from Fig. 5, that the response of the synchronization is directly affecting the performance of the PQ and current controller and consequently the operation of the entire RES. Therefore, the design of an enhanced GSC is essential to investigate how the accurate operation of the new DNαβ-PLL under harmonic distorted voltage and grid disturbances can beneficially affect the response of the GSC of a RES in terms of power quality.

The PQ controller is responsible for generating the reference currents under normal and faulty grid conditions. Under normal grid conditions, the generation of the reference currents is a conventional procedure [21, Ch. 9] and should be able to control the voltage of the DC-link ($V_{DC\text{-}link}$) and the active (P) and reactive (Q) power exchange. In case of balanced or unbalanced low voltage grid faults, the PQ controller is also responsible for the FRT operation of the RES [29]-[31]. This means that the generation of the reference currents should ensure a proper voltage and frequency support without any violation on the GSC converter ratings. The generation of the reference currents from the FRT method requires the definition of two important ratios. The first one is defined by $k_{VF} = Q'/P'$ and determines the ratio between the voltage and the frequency support. During the fault, the generated apparent power is considered as constant from the RES and therefore, through the ratio k_{VF} the reference active (P') and reactive (Q') power for the GSC control can be calculated. The ratio k_{VF} is usually defined within the grid codes for interconnecting RES and is dependent on the voltage sag of the faulty grid at the PCC. The second ratio k_{PN}, which is defined in (14), regulates the current injection between the full positive (k_{PN}=1) and the full negative sequence (k_{PN}=0) and is dependent on the target of the FRT strategy.

$$k_{PN} = \frac{\left|\boldsymbol{i}^{*}\right| - \left|\boldsymbol{i}^{-1*}\right|}{\left|\boldsymbol{i}^{+1*}\right| - \left|\boldsymbol{i}^{-1*}\right|} \tag{14}$$

Usually a full positive sequence current injection is chosen to support the faulty grid, but in some cases, the injection of negative sequence currents can be useful in the FRT strategy in terms of compensating the unbalanced grid conditions.

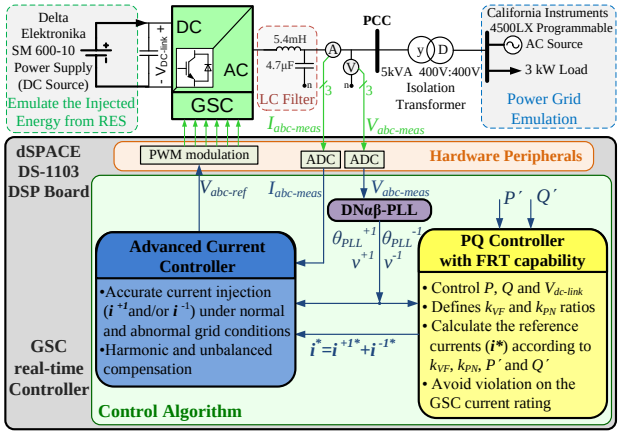


Fig. 5. Schematic of the experimental setup and the diagram of the advanced controller for the grid-connected RES

The reference currents ($\boldsymbol{i}^{*}$) can be calculated based on the active and reactive power references and on the positive and negative voltage vector as defined in (15)-(17) according to the instantaneous power theory [32].

$$\boldsymbol{i}_{\boldsymbol{P}}^{+1*} = k_{PN} \cdot \frac{P'}{\left|\boldsymbol{v}^{+1}\right|^{2}} \boldsymbol{v}^{+1} \quad \& \quad \boldsymbol{i}_{\boldsymbol{Q}}^{+1*} = k_{PN} \cdot \frac{Q'}{\left|\boldsymbol{v}^{+1}\right|^{2}} \boldsymbol{v}_{\perp}^{+1} \tag{15}$$

$$\boldsymbol{i}_{\boldsymbol{P}}^{-1*} = (1-k_{PN}) \cdot \frac{P'}{\left|\boldsymbol{v}^{-1}\right|^{2}} \boldsymbol{v}^{-1} \quad \& \quad \boldsymbol{i}_{\boldsymbol{Q}}^{-1*} = (1-k_{PN}) \cdot \frac{Q'}{\left|\boldsymbol{v}^{-1}\right|^{2}} \boldsymbol{v}_{\perp}^{-1} \tag{16}$$

$$\boldsymbol{i}^{+1*} = \boldsymbol{i}_{\boldsymbol{P}}^{+1*} + \boldsymbol{i}_{\boldsymbol{Q}}^{+1*} \quad \& \quad \boldsymbol{i}^{-1*} = \boldsymbol{i}_{\boldsymbol{P}}^{-1*} + \boldsymbol{i}_{\boldsymbol{Q}}^{-1*} \Rightarrow \boldsymbol{i}^{*} = \boldsymbol{i}^{+1*} + \boldsymbol{i}^{-1*} \tag{17}$$

where $\boldsymbol{i}_{\boldsymbol{P}}^{+1*}$ and $\boldsymbol{i}_{\boldsymbol{Q}}^{+1*}$ define the positive sequence active and reactive power components of the reference current vector respectively and the $\boldsymbol{i}_{\boldsymbol{P}}^{-1*}$ and $\boldsymbol{i}_{\boldsymbol{Q}}^{-*}$ the corresponding negative sequence components. The positive sequence voltage vectors can be defined as $\boldsymbol{v}^{+1}=v_d^{+1}+jv_q^{+1}$ and the 90° lagged version of it as $\boldsymbol{v}_{\perp}^{+1}=v_q^{+1}-jv_d^{+1}$. Correspondingly, the negative sequence voltage vectors can be defined as $\boldsymbol{v}^{-1}=v_d^{-1}+jv_q^{-1}$ and the 90° lagged version as $\boldsymbol{v}_{\perp}^{-1}=v_q^{-1}-jv_d^{-1}$. The voltage vectors are available on the GSC controller through the proposed PLL. The FRT algorithm is also in charge to maintain the injected currents within the converter ratings, especially under low-voltage grid faults. In case of violation on the GSC ratings, the reference currents should be modified in a way to maintain the k_{VF} and k_{PN} ratios and to ensure a proper limitation of the injected currents.

Since the reference currents have been calculated, the current controller has to ensure the proper injection of high quality currents in the power grid. This is not a trivial aspect when positive and/or negative sequence currents should be injected under unbalanced and harmonic distorted voltage. Advanced current control techniques are required to enable the high quality current control under abnormal grid conditions, like suggested in [33]-[39]. For the purposes of this paper, the current controller presented in [33] has been implemented, which requires a simplified structure and can achieve a high quality positive or negative current injection under faulty and distorted grid voltage. The selected current controller is a simplified solution with low control efforts. It consists of a conventional current controller enhanced with harmonic [40] and unbalanced [33] compensation modules and can achieve a high quality positive or negative sequence current injection under normal conditions and under unbalanced grid faults.

The structure of the enhanced GSC controller that has been developed is presented in Fig. 5. The implemented GSC controller achieves proper and high quality operation even under grid faults and harmonic distorted voltage. This GSC will be used on the investigation of the effect of the accurate synchronization on the RES performance in the next section.

IV. Simulation and Experimental Results

The new synchronization method has been proposed in Section II and an advanced GSC controller has been implemented in Section III. Simulation and experimental results will be presented in this section regarding the response of the new DNαβ-PLL under harmonic distorted voltage and several grid disturbances. Furthermore, the beneficial effect of

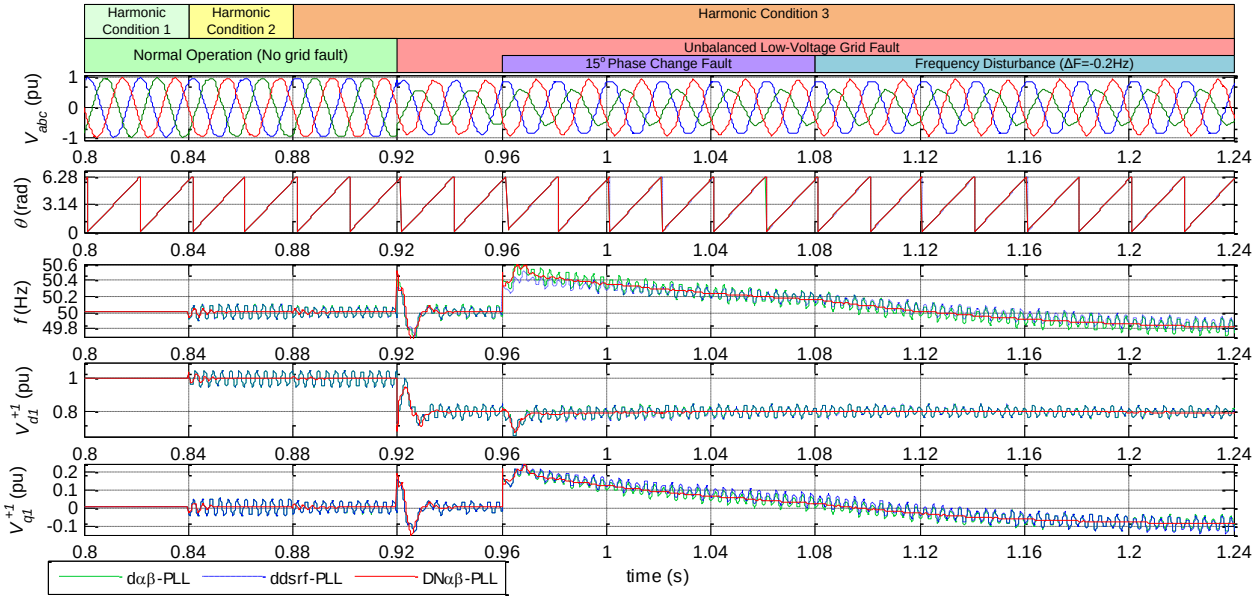


Fig. 6. Simulation results comparing the PLL response of the new DNαβ-PLL, the ddsrf-PLL, and the dαβ-PLL under several abnormal grid conditions.

accurate synchronization, through the new DNαβ-PLL, on the performance of the grid-connected RES is also investigated. This innovative investigation proves the significant impact of the accurate synchronization on the response of the RES and demonstrates the considerable enhancement of the power quality of the RES due to the proposed DNαβ-PLL.

A. Experimental Setup

An experimental setup has been implemented to verify the work presented in this paper. The experimental setup is considering the response of the new synchronization method and the effect on the performance of GSC control of a RES. A Delta Elektronika Power Supply (SM 600-10) operates as a DC source to emulate the energy produced from the RES and a Danfoss FC302 2.2 kW inverter acts as the GSC. A California Instruments 4500LX programmable AC source in combination with a parallel connected 3 kW load is used to emulate the power grid. For the experimental investigation presented in this section, the PLL algorithm and the enhanced control of the GSC have been designed using a dSPACE DS1103 DSP board in combination with the dSPACE Control Desk and Matlab/SIMULINK Real Time Workshop. The sampling rate and the switching frequency of the designed GSC controller have been set to 7.5 kHz. The schematic of the experimental setup is presented in Fig. 5. The exact same setup has been implemented as a simulation model in Matlab/ SIMULINK to ensure the proper operation of synchronization and GSC control before applying them on the real system.

B. Response of the new synchronization method

The DNαβ-PLL aims to achieve a robust and accurate operation under a harmonic distorted grid without affecting the dynamic synchronization response in case of grid faults.

A simulation case study presented in Fig. 6 provides a comparison between the response of the DNαβ-PLL, the dαβ-PLL [19], and the ddsrf-PLL [18] (all PLLs are set according to the same tuning conditions as explained in Section II). It is obvious that the proposed PLL achieves an accurate response under highly distorted grid voltage, where the Harmonic Conditions (HC) 1-3 are explained in Table IV. The ddsrf-PLL and dαβ-PLL present similar dynamic performance, but their accuracy is affected by the harmonic distortion. Moreover, Fig. 6 demonstrates that the accurate response of the new PLL is achieved without affecting the dynamic performance of the synchronization since the DNαβ-PLL presents a similar dynamic response with the dαβ-PLL and ddsrf-PLL under several faults. The proper and robust performance of the new PLL is verified under an unbalanced low-voltage grid fault (Type D with a voltage sag (*d*) of 37% [41]), a 15° phase shifting fault and a frequency step of -0.2 Hz. The appropriate performance of the proposed PLL is also experimentally validated under harmonic distorted voltage and unbalanced grid fault as shown in Fig. 7. The experimental

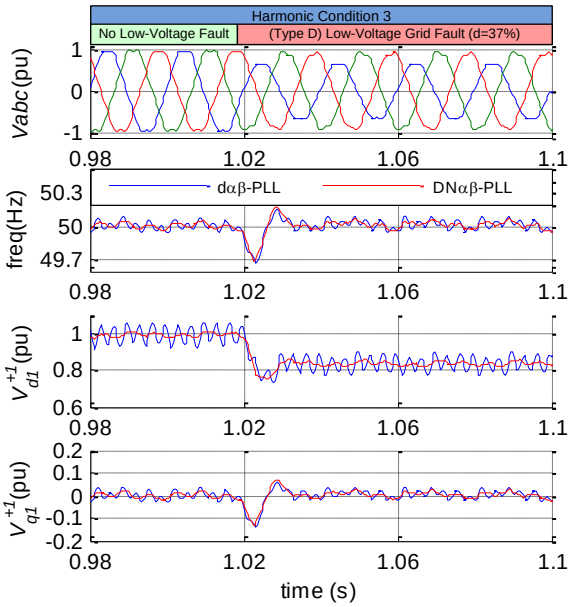


Fig. 7. Experimental results presenting the accurate response of the new DNαβ-PLL under harmonic distorted and unbalanced grid votlage.

results prove the accurate and dynamic response of the new PLL under harmonic distorted voltage and grid disturbances.

Synchronization methods based on MAF [22]-[24] are simplified regarding the complexity (Table II) and can achieve accurate performance under unbalanced and harmonic distorted voltages. A MAF-PLL [22]-[23] inherits the structure of the conventional dq-PLL [9] and uses a MAF to clear out the oscillations caused by harmonics and unbalance conditions. A modified MRF-PLL [22], [24] inherits the structure of the multi reference frame ddsrf-PLL [18] and replaces any low pass filters with a corresponding MAF to improve its filtering capabilities against harmonics and unbalanced conditions. The accuracy of these PLLs can be slightly affected when the operating frequency deviates from the nominal value due to the discrete implementation of the MAF. Even if these inaccuracies are overcome by using a variable sampling rate [25] (which is not an indicative solution in many control applications) the main disadvantage of these PLLs is the slow dynamic performance. Therefore, a performance comparison between the proposed PLL, the MAF-PLL and the modified MRF-PLL is presented in Fig. 8 and Table III. For the purpose of this comparative analysis the three PLLs are tuned according to [22]. The simulation results show that these PLLs are accurate under nominal operating

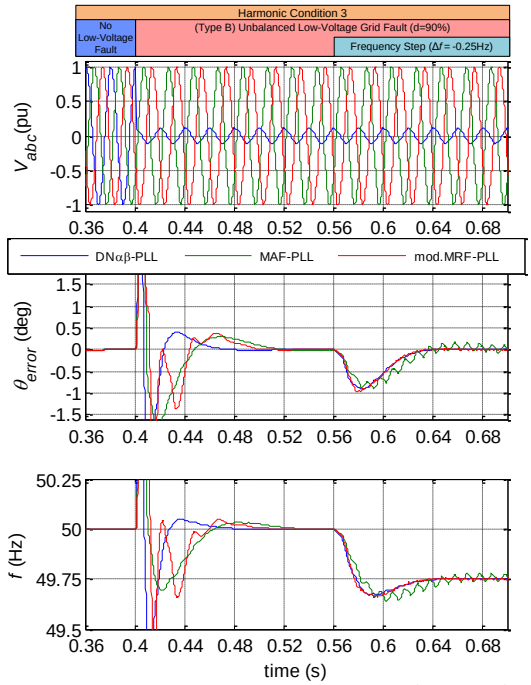


Fig. 8. Simulation results comparing the performance of the DNαβ-PLL and two MAF based PLLs under harmonic distorted and unbalanced voltages.

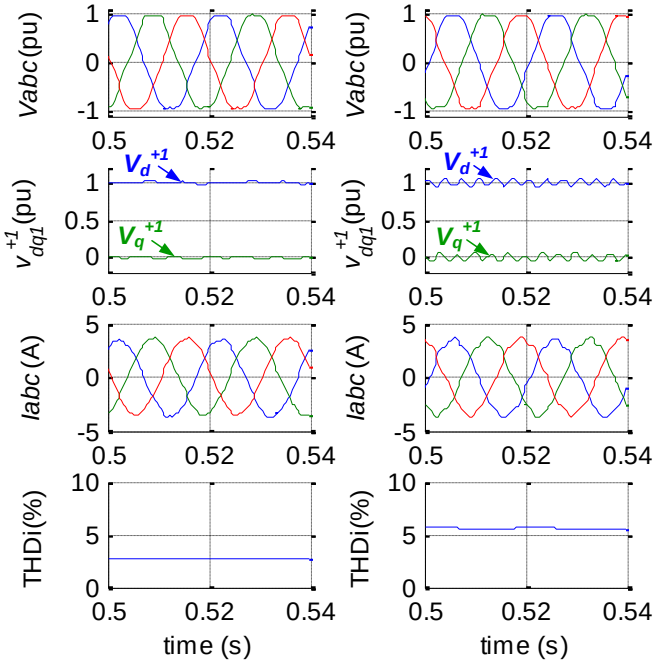
TABLE III
SUMMARY OF THE RESULTS OF FIG. 8

Grid Conditions	MAF-PLL	mod.MRF-PLL	DNαβ-PLL
Harm. Distort. & f=50 Hz	√	√	√
Harm. Distort. & **a Voltage Sag occurs**	**slow**	**slow**	**fast**
• Settling Time (θ_{error}<0.1°)	99.7 ms	89 ms	57 ms
• Peak-Peak Phase error at 50 Hz	0 °	0 °	0 °
• Peak-Peak Freq. error at 50 Hz	0 Hz	0Hz	0Hz
Harm. Dist./Unbalanced & **Freq. Step**			Fast & accurate
• Settling Time (f_{error}<0.01 Hz)	130 ms	74 ms	70 ms
• Peak-Peak Phase error at 49.75 Hz	0.19 °	0.05 °	0 °
• Peak-Peak Freq. error at 49.75 Hz	0.041 Hz	0.012 Hz	0 Hz

frequency, harmonic distorted and unbalanced voltage. The frequency deviation from the nominal value in combination with the harmonic and unbalanced grid conditions can cause inaccuracies on the estimated signal of MAF-PLL as shown in Fig. 8 and Table III. The enhanced filtering capability of the modified MRF-PLL, especially for the oscillations caused by the negative sequence, significantly minimize the inaccuracies under a non-nominal frequency operation. On the other hand, the accuracy of the proposed DNαβ-PLL is not affected by the harmonic distortion, the unbalanced conditions, and the frequency deviation. In addition, the new PLL presents a significantly faster dynamic performance compared to the PLLs based on MAF as demonstrated in Fig. 8 and Table III, especially under low-voltage grid faults. The fast dynamic operation of the new PLL is particularly important for the proper FRT operation of RES under grid faults. Therefore, the increased complexity of the proposed PLL (Table II) is paid back by a very accurate and fast synchronization performance.

C. *RES performance when using the proposed PLL*

The results, presented in Fig. 6 and Fig. 7, show that the proposed PLL achieves an accurate synchronization and the oscillation-free estimation of the synchronization signals (θ *and* $v_{dq_1}^{+1}$). As shown in (15)-(17), the synchronization signals are used from the PQ controller to generate the reference currents. Additionally, the operation of the current controller [33] is based on an accurate estimation of the synchronization signals so it is expected that the accurate synchronization is directly affecting the GSC control and as a consequence the performance of the RES. An experimental investigation is presented here to prove how the accurate synchronization through the proposed PLL can enhance the



(α) RES response (with DNαβ-PLL) (b) RES response (with dαβ-PLL)

Fig. 9. Experimental results for the performance of the RES under harmonic distorted voltage, when using (a) the proposed DNαβ-PLL and (b) the dαβ-PLL for the synchronization of the GSC.

TABLE IV
THE IMPACT OF THE ACCURATE SYNCHRONIZATION THROUGH THE PROPOSED SYNCHRONIZATION ON THE POWER QUALITY OF RES

Grid Operating Conditions			Synchronization Method	
			dαβ-PLL	DNαβ-PLL
Low Voltage Fault	Voltage Harmonic Distortion	Freq (Hz)	THD(%) of the injected currents	
No Fault	HC-1	50	2.45	2.45
No Fault	HC-2	50	5.60	2.60
ULVF-1	HC-2	50	6.50	4.00
ULVF-1	HC-2	49.5	6.65	4.20
No Fault	HC-3	50	5.10	2.90
ULVF-1	HC-3	50	6.05	4.40
ULVF-1	HC-3	49.5	6.30	4.55

Index:
- ULVF-1: Type D Unbalanced Low Voltage Fault with d=37%
- HC-1: Harmonic Cond. 1 (High-frequency harmonics (HFH)=0.1%)
- HC-2: Harmonic Cond. 2 (THD_V=5% with $|V_5|$=4.9%, HFH=0.1%)
- HC-3: Harmonic Cond. 3 (THD_V=4.57% with $|V_5|$=4%,$|V_7|$=2%, HFH=0.1%)
- HC-4: Harmonic Cond. 4 ($|V_5|$=6%, $|V_7|$=5%, $|V_{11}|$=3.5%, $|V_{13}|$=3%, $|V_{17}|$=2%, $|V_{19}|$=1.5%, $|V_{23}|$=1.5%, $|V_{25}|$=1.5%, $|V_{19}|$=1.5%, HFH=0.1%)

power quality of the RES.

The steady state performance of the grid-connected RES based on experimental results is presented in Fig. 9 under a highly harmonic distorted grid voltage (with harmonic condition 2 (HC-2) as explained in Table IV). Fig. 9(a) demonstrates the RES performance when the proposed DNαβ-PLL is used for the synchronization. It is shown that the new PLL estimates accurately the synchronization signals and therefore the reference currents are generated without any oscillations due to the harmonic distortion. Therefore, the RES achieves to inject high quality currents with a total harmonic distortion (THD_i) of 2.6%. On the other hand, Fig. 9(b) presents the RES operation when the RES uses the dαβ-PLL for the synchronization. The inaccuracies of the dαβ-PLL, caused by the harmonic distortion, raise oscillations on the synchronization signals and therefore, the generated reference currents and the operation of the current controller are affected. Consequently, the RES with a non-robust synchronization against harmonics presents a low quality current injection with a THD_i of 5.6% (outside of the grid code limits) under harmonic distorted grid voltage. This experimental case study proves that the accurate synchronization is a key aspect for the power quality of the RES. A further experimental investigation to prove the beneficial effect of the accurate synchronization on the power quality of the RES is summarized in Table IV. Table IV compares the power quality of the RES when using a robust and a non-robust synchronization method under several harmonic conditions and several grid faults. It can be seen that the accurate operation of the proposed PLL enhances the RES performance and enables a high quality current injection under any grid conditions. The experimental results of Table IV prove the significant contribution of the proposed DNαβ-PLL in the power quality of grid-connected RES.

The dynamic response of the GSC is a critical aspect, especially under low-voltage grid faults, where the RES should immediately support the faulty grid [1]-[4]. The fast

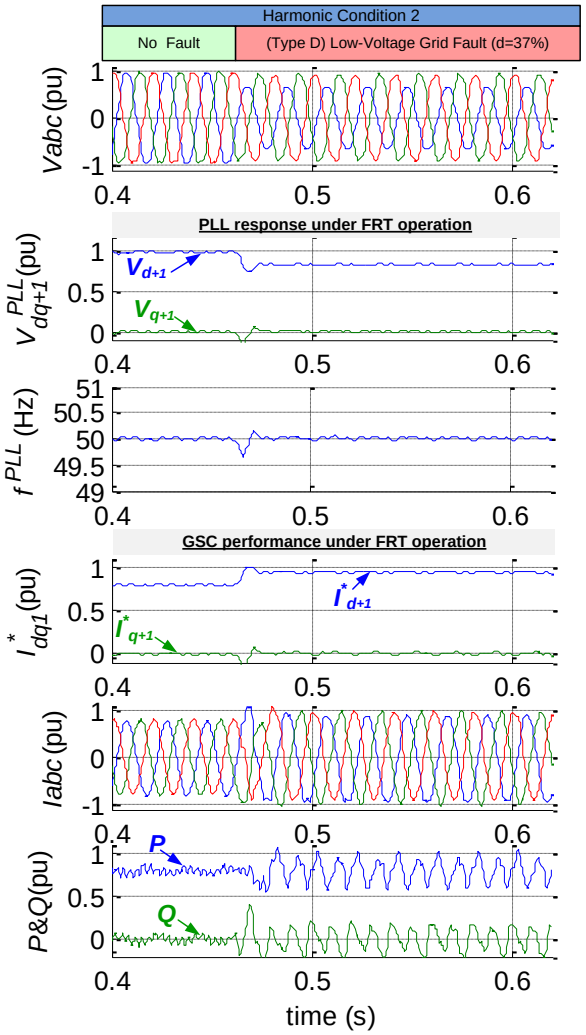


Fig. 10. The FRT performance of a grid-connected RES, when the new DNαβ-PLL is used for the synchronization, under unbalanced grid fault and harmonic distorted voltages.

response of the RES, when a fault occurs, is directly affected from the dynamic performance of the synchronization. The proposed PLL achieves an accurate response under harmonic distorted voltage without compensating its dynamic response, as proven in Figs. 6-8. Thus, it is important to prove that the proposed DNαβ-PLL can enable the proper dynamic FRT performance of the RES when a fault occurs in order to meet the grid regulations. The experimental case study presented in Fig. 10 shows the RES performance when operating under harmonic distorted voltage (harmonic condition 2 as shown in Table IV) and an unbalanced low-voltage grid fault occurs. The RES is operating in the 80% of the GSC ratings before the low-voltage fault. When the fault occurs, the proposed DNαβ-PLL ensures the accurate and fast estimation of the synchronization signals as shown in Fig. 10. The proper synchronization enables the fast and adequate FRT operation of the PQ control algorithm to ensure the full positive current injection (k_{PN}=1), the support of the grid with k_{VF}=0, and the limitation of the current injection within the converter limits.

V. CONCLUSIONS

The proposed DNαβ-PLL achieves an accurate, dynamic and robust synchronization under harmonic distorted voltage and under several grid disturbances. The real time execution of the new synchronization method requires significantly less processing time compared to other PLLs with equivalent response. The robust and accurate response of the new PLL enhances the RES performance by improving the power quality of the injected currents and by enabling the proper FRT operation under grid disturbances.

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